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The Evaluation of Device Model Dependence in the Design of a High-Frequency, Analog, CMOS Transconductance-C Filter

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THESIS APPROVAL

The abstract and thesis of Susan Rose Brotman for the Master of Science in Electrical and Computer Engineering were presented May 6, 1994, and accepted by the thesis committee and the department.

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ABSTRACT

AN ABSTRACT OF THE THESIS OF Susan Rose Brotman for the Master of Science in Electrical and Computer Engineering presented May 6, 1994.

Title: The Evaluation of Device Model Dependence in the Design of a High–Frequency, Analog, CMOS Transconductance–C Filter.

It is important to have the ability to predict the effects of device model variation when designing integrated transconductance–C type active filters. Applying these filters to integrated circuit design has become increasingly popular due to its ease of implementation in monolithic form. With the introduction of fully automated design tools, predictable behavior of high–level variables becomes still more important. The purpose of this study is to evaluate the process parameter spread of analog device models to determine the effect on the design parameters of an active filter. This information's significant contribution directly effects the feasibility and realization of automating analog filter design.

In order to explore the dependence of filter performance on the device model parameter spread, a fifth–order inverse Chebyshev filter is designed and simulated using a two year history of process models. It has not been observed that higher order filters have been successfully designed using fully automated design tools. This filter was realized using automated filter design software

currently being developed in parallel with this study. A single–ended input to single–ended output transconductance amplifier is chosen for this design for its simplicity and small size. Differential performance is easily adapted with exact duplication which is demonstrated in the measurements of the fabricated filter.

Simulation of the design is performed using MOSIS SCNA device parameters. Filter performance data such as cutoff frequency, stopband attenuation, and phase response is collected. Experimental results from the fabricated device are compared to simulation and the original prototype.

It is shown that the most predicable effect on the design parameters of a filter is caused by the parasitic output conductance parameter g_o. This process dependent variable causes both a deviation in the cutoff frequency, and a decrease in the filter quality factor. In addition, it is also shown that the practice employed to predistort for absorption of parasitic capacitors in a MOS technology is a very effective tool in the reduction of capacitive process dependence.

THE EVALUATION OF DEVICE MODEL DEPENDENCE IN THE DESIGN OF A HIGH–FREQUENCY, ANALOG, CMOS TRANSCONDUCTANCE–C FILTER

by

SUSAN ROSE BROTMAN

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Portland, Oregon
May 1994

Susan Rose Brotman

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER I

INTRODUCTION

OVERVIEW

It is important to have the ability to predict the effects of device model dependence when designing analog transconductance–C (g_m–C) type filters. Application of these filters to integrated circuit design has become increasingly popular due to its ease to implement in monolithic form [1–4]. With the introduction of fully automated design tools, predictable behavior with regard to high–level variables becomes still more important. The purpose of this study is to evaluate the process parameter spread of analog MOSFET models to determine the effect on the design parameters of a filter. This information's significant contribution is aimed towards the realization and feasibility of automating analog filter design. This chapter defines the importance of process dependent device model research with special regard to integrated g_m–C circuits. A review of literature indicates the importance of device model parameters in a broad range of current integrated circuit designs and applications. A review of low–pass filter applications and key specifications provides a foundation for understanding filter performance characteristics. Test figure selection and method of realization is now introduced. In closing, the limitations of this research study are described.

Integrated Circuit Process Parameter Dependence

Technological advances in the complexity and versatility of integrated circuits continues to grow rapidly. Higher level design languages have shifted the limitations of advancement of integrated circuits from the development of conceptual designs to the technological limitations of physical realization. That is, circuit designs are developing in complexity faster than the process technology required to fabricate them.

The integration of g_m–C continuous–time filters into microelectronic devices has several desirable characteristics including some of those inherent to the previously discrete method of realization. First, all elements of the filter can be realized on a silicon substrate. Operational simulation of inductive, capacitive and resistive elements can all be implemented on a very small silicon area with low power consumption. The space ⇆ power tradeoff may be questioned. The use of discrete elements use less power, (no active devices); however, power usage in this CMOS application is normally quite a small cost. Second, not only can integrated active devices simulate the LC ladder behavior, they also inherit excellent passband sensitivity properties. The discrete inductor and capacitor in an LC ladder structure have a component sensitively directly proportional to the change or slope of the overall circuit transfer function. This relationship would imply a low sensitivity value of component tolerance variations in a structure with a maximally flat passband characteristic. In the same respect, it is expected that simulation with active devices would also exhibit this property. The inductor's behavior can functionally be defined by the equation,

$$L = \frac{C_L}{g_m^2}$$

which uses only capacitor and transconductance element values. As integrated elements, the sensitivity equates directly to process parameters. For the capacitor, this would depend on the method of capacitor realization. Specific to this research is the variation with respect to the poly1/poly2 unit capacitance level. The g_m magnitude has several process parameter dependencies and at present, an unavoidable tolerance band. Primary process parameters are threshold voltage, V_T, body effect parameter, γ, surface mobility, μ, and oxide thickness, t_{ox}. Fortunately, the ability to fine tune the g_m value of the gain element comes from its proportionality to device bias current. The importance of this electrically tunable property is observed in the time constant relationship,

$$\frac{1}{\tau} = \omega = \frac{g_m}{C}$$

From this equation, and L above it is obvious that the frequency performance of a filter is dependent on process dependent elements. While the absolute values within the same die may vary, very accurate process dependent parameter ratios can be attained [5]. Also important is that while process variations, time, and temperature may effect the absolute value, the ratio relationship is maintained. An implication of this relationship is that frequency becomes a matter of a scaling factor or multiplication by a constant.

Finally, LC ladder simulation with transconductors and capacitors also generates a dimensionless selectivity or pole quality factor, Q. A high value of Q translates to a steep transition band. In a common two–integrator or second–order configuration, this quality factor is characterized as

$$Q = \sqrt{\frac{g_{m1}\, C_1}{g_{m2}\, C_2}} \quad .$$

From this equation it is obvious that the selectivity response of an active filter is dependent on a ratio relationship of elements.

The characteristic of a scaling factor offers a significant advantage for g_m–C filter design. Developed in a frequency and element normalized fashion, response can then be made process specific simply by the multiplication of all filter elements by a known *process dependent constant!*

Review of Literature

Process dependent parameters have been evaluated for their effects on analog circuit performance in a broad range of areas. The necessity to reduce power along with silicon area requires the investigation of process variation effects on low–voltage operation of CMOS integrated circuits [6]. Great strides continue in the direction towards miniaturization and portability. Advanced integrated circuit designs that perform the functions of larger, discrete components are ideal blocks for this integration. Growth continues globally in the fields of space exploration and satellite utilization for communications. These ventures use massive amounts of high performance, high reliability microelectronic circuits. These elements are often subjected to high levels of radiation, hence the effects of process variations on irradiated microelectronic circuits has also been studied [7].

Mass production of integrated circuits has allowed their utilization in low end electronic devices across the board. Process variations, to some degree, have always been present. To gain a better insight of these tolerance effects,

device parameters have been scrutinized for their independent and correlated intra–die behavior [8,9], i.e., MOS transistor mismatching [10]. On a higher level, process parameters have also been evaluated for inter–die statistical modeling to aid in yield estimations [9]. Acceptance of the model depends on performance specifications of the circuit. All findings report that a concrete understanding of the key parameters of the MOSFET device is essential.

On another high level, but separate thread, it has been shown that the distorted frequency response of an Operational Transconductance Amplifier–Capacitor filter can be predicted as a function of the nonlinearities of the OTA [11]. This study analyzed a model of the distorted transfer function of the filter, without regard to the lower level device model parameters. Nonlinearities were assumed to be caused by large signal amplitude.

It is intended here to determine if a high level of pre–sort can be determined which in fact is a combination of the key concepts examined in [9] and [11]. That is, can it be predetermined whether or not a specific device model will qualify for a given g_m–C filter's design specifications. This filtering is a function of frequency not signal amplitude. Non–modeled capacitance variation effects are also investigated for significant effects on continuous–time performance.

Applications of Low–pass Filter Design

Applications for analog, high–frequency, CMOS filters are expanding in scope. Digital data transmission rates continue to be pushed upward in the frequency spectrum and multimedia communications are steadily becoming a reality. This trend shows a need for high performance devices that are reliable in the transmission of digital data and video signal reconstruction. In an analog

real world environment with digital technological developments, interfacing converters will always be required.

Basic signal theory shows that frequency response is often measured by magnitude and phase. Assuming a sinusoidal signal, where ω is some test frequency, the input signal is denoted as

$$v_i = V_i \sin(\omega t) \quad ,$$

and the output signal as,

$$v_o = V_o \sin(\omega t + \phi) \quad .$$

The filter response is then completely described by its magnitude response,

$$|H(\omega)| = \frac{V_o}{V_i} \quad ,$$

and its phase response,

$$\angle H(\omega) = \phi \quad .$$

The transfer function is a gain ratio of the output amplitude to the input amplitude of the device and is often expressed in decibels where,

$$\text{Gain dB} = 20 \log |H(\omega)| \quad .$$

A review of elementary communication theory provides one relevant application for the analog low pass filter. Nyquist's sampling rate is defined as $2 \cdot B$ samples per second, where B is the highest frequency component or the band limiting frequency of the signal. If the transmitted signal is under sampled, that is at a rate below the Nyquist rate, overlapping of signal tails occurs. This spectral folding or aliasing causes signal distortion which makes the original signal impossible to recover. Lowpass filters, with the transfer function characteristics shown by the dotted line Figure 1, are frequently used in

anti–aliasing applications [12]. This has the corrective effect of reducing the error signal energy of the signal by cutting off the tail ends before sampling.

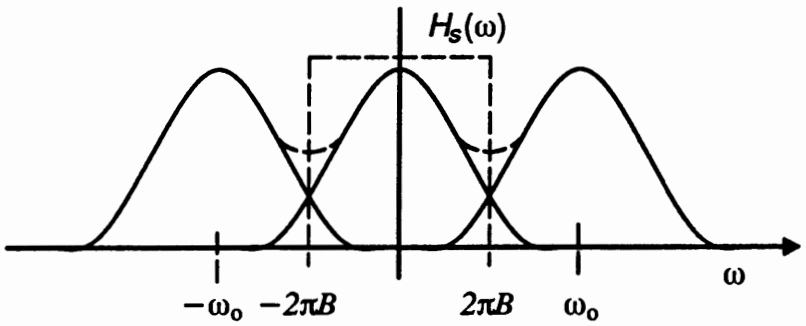


Figure 1. Low–pass filter anti–aliasing example

This function would be performed on the input of a sampled–data filter, such as a switched–capacitor (SC) filter. This low–pass filter also limits high–frequency input noise which would otherwise be added to the resulting signal. On the output side of an SC filter, a continuous–time low–pass filter is commonly used to smooth out or further attenuate unwanted high frequency components. Important design specifications of this type filter are flat passband attenuation along with steep roll off or a narrow transition band.

The phase response, just as the magnitude response, is also important in transmission circuits and systems. Nonlinearities in phase may also cause distortion of transmission information. Frequently, phase, ϕ, is defined in terms of delay. A filter's ideal phase response should be linear over a band of frequencies or delay should be constant. That is,

$$T_d(\omega) = T_o \ , \qquad \phi(\omega) = -\omega T_o \ .$$

If variations of group delay occur in a video signal, for example, visual impairment of the signal will occur depending upon which portion of the signal

spectrum is affected. For example if luminance and chrominance have a difference in delay, then misregistration of a color with picture detail will occur. Delay characteristics are also important in transmission of digital data, such as with time dependent square wave pulse transmission. Phase distortion create erroneous information as phase and amplitude are interrelated . Pulse dispersion or pulse spreading occurs when either the magnitude or the delay characteristics are not ideal. This distortion of pulse shape creates cross talk in time–division multiplexed systems and distortion of each signal's frequency spectrum in a frequency–division multiplexed system. An important filter design characteristic which would minimize these types of effects would be a flat delay response across the frequency band of interest.

Tolerance plots of the important filter characteristic's thus far defined would have the shape of the plots in Figure 2.

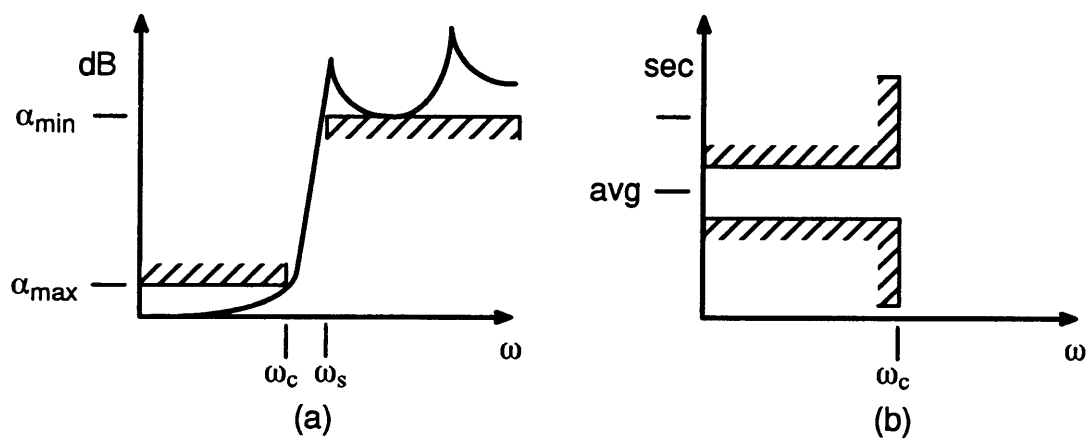


Figure 2. Filter tolerance plots: (a) Attenuation, (b) Group delay

Test Figure Selection and Realization

In order to explore the dependence of filter performance on device model parameter spread, a fifth–order inverse Chebyshev filter is designed. This is a

low Q, low–pass filter, with maximally flat passband and equiripple stopband attenuation characteristics. It is a more efficient filter, in attenuation per pole, than the simpler, maximally–flat Butterworth, and also has the advantage of a steeper rolloff. It is also chosen in this project for its small delay variation feature. Although the delay is not as constant as the Bessel filter delay, the inverse Chebyshev, again, offers a steeper rolloff.

It is attempted to accurately produce this filter using automated filter design software currently being developed in parallel with this study [13]. It has not been observed that higher order filters have been successfully designed using fully automated design tools. Predistortion methods are employed to offset the CMOS inherent capacitors. A single–ended input to single–ended output transconductance amplifier [14, 15] is chosen for this design for its simplicity and small size. Differential performance is easily adapted by exact duplication on final IC layout.

Layout for fabrication is performed using Magic [16], an interactive tool for creating and modifying VLSI circuit layouts. All circuit simulations are performed using the extracted Magic circuit which includes parasitic capacitor values of 1fF or greater. Fabrication of final design is an analog technology, MOSIS , 2.0μm n–well CMOS process [17].

Limitations

This study is limited to the extent that only an LC ladder type filter with a low Q value is used to evaluate the process model dependence. In a practical, passive ladder filter structure, the series/parallel branch component values can be determined by a mathematically recursive process. This feature lends itself nicely to the field of active LC ladder filter design automation.

The low Q ($Q \leq 10$) may be a more important limitation. The Q factor, or quality factor also specifies the sensitivity of the filter. The closer the dominant pole is to the $j\omega$–axis, the higher the Q and the more selective the filter response. The two–integrator–loop biquadratic circuit or *biquad*, is an important building block in active filter design. It has been shown that these second–order sections with high Q are quite sensitive to small changes in dominate pole frequency, ω_p [18]. It is noted however, that variations of magnitude and phase response due to process variations will be present in any filter design, regardless of its realization or Q value.

A final limitation of this study is that only MOSIS analog, SCNA, 2.0μm technology is investigated. Many process dependent device parameters, whether independent or correlated to other process dependent parameters, are random variables whose behavior is described by a probability function. The variations of processes usually give rise to a *Gaussian* or *normal* distribution of device model parameters [5]. The source of the MOSFET device model parameters and poly1/poly2 capacitance units used in this research project is the NSF MOSIS IC fabrication ftp server. The ftp server archives a standard data file for each fabrication run that characterizes MOSFET AC and DC parameters and the inherent parasitics of a MOS process. The test group for this study is a set of eight MOSFET device models. It is not assumed to be a statistically valid sample. During the course of this study the MOSIS project continually made MOS device models available from more recent fabrication runs. Although not included in the model test group of this research project, newer models are examined by the same methods outlined and have displayed no significant performance deviations. TABLE XV of Appendix A, on page 75, identifies by MOSIS fabrication run name all of the MOS models tested.

CHAPTER II

METHODOLOGY OF INVESTIGATION

OVERVIEW

In order to evaluate the process parameter dependence on continuous–time filters, performance specifications are selected and a test figure is created. In order to limit systematic errors, diligent design techniques are implemented from the lowest levels. Research extends to cover the important idiosyncrasies of low level element design, mathematical versus more empirical variable values for capacitors, and the inclusion of predistortion and pre–emphasis techniques to ensure optimal analog performance. This chapter describes in detail the design process used to derive the final filter structure. Test techniques employed for the collection of filter performance data are also described.

CIRCUIT DESIGN

Transconductance Cell Design

The single–ended transconductance element shown in Figure 3

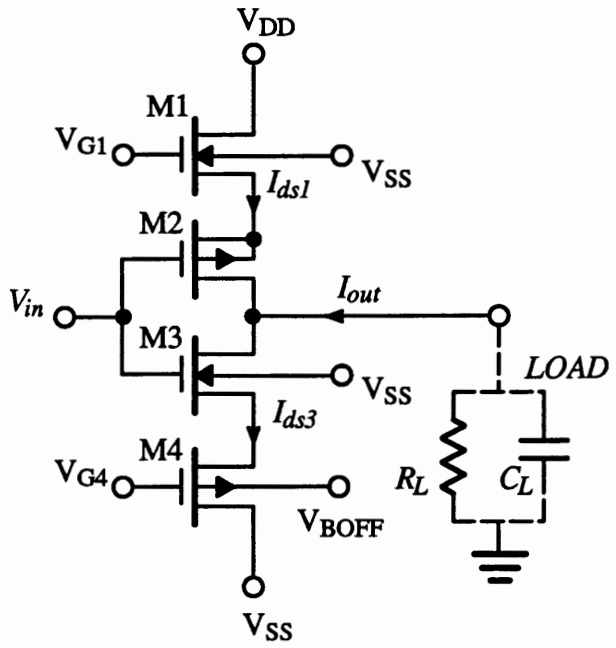


Figure 3. Inverting transconductance element

is chosen as the gain element for this design due to its small size and simplicity. Compared with a differential design, the single–ended design does have some important draw–backs. The differential design reduces signal crosstalk, increases linear operating range and has a higher power supply rejection. The ubiquitous coupling parasitics are also reduced in a differential design, which can be shown to be a great asset. The negative side of a differential design includes complexity of design, increased required Si real estate and higher power consumption concerns. Differential designs often require additional, bulky off–chip transformers [19, 20]. It is expected that differential operation can be

accomplished by exact duplication of the single–ended filter structure. In theory, this should make available most of the additional features of the differential device.

Design of the individual g_m cell is known to be dependent on process parameters [2,14, 21]. From the onset of optimizing aspect ratios for best linear range of operation and best frequency response, variables such as γ, the body effect or threshold voltage parameter, and λ, the channel–length modulation parameter, play a role. Basic theory of MOSFET operation, neglecting these low level process variations, can be characterized by the following square law model equations [14, 22]. Knowing that $I_{ds1} = I_{ds2}$, $I_{ds3} = I_{ds4}$, and that the devices are operating in the saturation region,

$$I_{out} = I_{ds1} - I_{ds3}$$

$$I_{ds1} = K_{eff} \cdot \left(V_{G1} - V_{in} - V_{tn1} - |V_{tp2}|\right)^2$$

$$I_{ds3} = K_{eff} \cdot \left(V_{in} - V_{G4} - V_{tn3} - |V_{tp4}|\right)^2$$

where

$$K_{eff} \therefore \frac{K_n \cdot K_p}{\left(\sqrt{K_n} + \sqrt{K_p}\right)^2} \quad .$$

This equation reflects the composite nature of the N and P transistor pair. Defining

$$\Sigma V_T = V_{tn1} + V_{tn3} + |V_{tp2}| + |V_{tp4}| = 2 \cdot V_{Tc}$$

and

$$\Delta V_T = \left(V_{tn3} - V_{tn1}\right) + \left(|V_{tp4}| - |V_{tp2}|\right) + \left(V_{G1} - V_{G4}\right),$$

$$I_{out} = -K_{eff} \cdot \left(V_{G1} + V_{G4} - \Sigma V_T\right) \cdot \left(2V_{in} - \Delta V_T\right) \quad .$$

If $V_{BS} = 0$, and the gate biases V_{G1} and V_{G4} are equal then,

$$\left(V_{tn3} - V_{tn1}\right) = \left(\left|V_{tp4}\right| - \left|V_{tp2}\right|\right) = 0$$

and

$$\left(V_{G1} - V_{G4}\right) = 0 \ .$$

Then

$$\Delta V_T = 0 \quad ,$$

and I_{out} reduces to

$$I_{out} = - K_{eff} \cdot \left(2V_G - \Sigma V_T\right) \cdot \left(2V_{in}\right) \quad .$$

Defining

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{V_{ds}} = - 2K_{eff} \cdot \left(2V_G - \Sigma V_T\right) \quad ,$$

or

$$g_m = - 4K_{eff} \cdot \left(V_G - V_{Tc}\right)$$

and

$$I_{out} = - g_m \cdot V_{in} \quad .$$

Variations in g_m or tuning ability are normally obtained by varying V_{G1}, while DC offset nulling can be implemented by varying V_{G4}. In this design, a separate biasing circuit was employed to negate the DC offset created by the nonzero V_{BS} of M4. An extensive numerical derivation is presented in [14] and need not be repeated here. In brief, the DC offset is created in an identically sized sensing circuit. It is then inverted and applied back to the bulk or back gate of M4, (V_{BOFF}). Simulation proved this method to be quite effective in reducing the body effects of the circuit. Circuit schematic is included in Appendix D on page 91.

The g_m of the MOS transistor can be stated in terms of bias current I_{ds}. Neglecting λ, this relationship is

$$g_m = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_{ds}} \quad .$$

As previously stated, symmetry is implied between the upper and lower transistor pairs. Therefore, ideally, g_m is the same for all transistors. Optimum sizing for linearity is derived by solving these relationships for W_p, W_n, L_p, and L_n.

$$\frac{W_n}{L_n} = \frac{g_m^2}{\sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \frac{W_n}{L_n} \cdot I_{ds}}} \quad ,$$

and with typical n–type carrier mobility approximately three times that of p–type carrier mobility,

$$\frac{\mu_n}{\mu_p} = 3 \quad ,$$

which leaves

$$\frac{W_p}{L_p} \simeq 3 \cdot \frac{W_n}{L_n} \quad .$$

Minimum sized devices are chosen for the highest frequency response. Choosing $L_p = L_n$, and simulating several MOSFET models for best average linearity, final aspect ratio for n–channel is 8/2 and for the p–channel, 20/2. All sizes are in microns (μm). This gives a working g_m of approximately 150μS and a cutoff frequency above 100MHz.

Simulation of an LC Ladder

In any lowpass filter design, the passband behavior is an important specification to meet. The low passband sensitively of the LC ladder topology is an important consideration for this study of performance versus process

variation. The ability to electronically tune the active filter g_m to overcome process variations is available in this design. However, for study purposes, no tuning is performed. The low passband sensitivity advantage of the LC ladder is therefore quite desirable.

The transmission characteristics of an inverse Chebyshev filter can be specified by four parameters. These specifications are passband edge, ω_c; stopband edge, ω_s; maximum passband attenuation, α_{max}; and minimum stopband attenuation, α_{min}. The more stringent the filter specifications, the closer the response of the filter is to ideal. The cost is higher order and higher design complexity. For this design, the original specifications were –3dB, at 18MHz, (F_c) and –40dB at 30MHz (F_s). Preliminary simulations performed on layout extracted circuits showed that the original specifications were too tight for the prescribed method of filter realization and available g_m cells. Parasitic effects required a pre–emphasis of the stopband attenuation. Considering the physical restriction of limited chip area, in order to maintain the original order of the filter, the stopband frequency was increased to 36MHz, a modest change.

Minimum filter order necessary to realize a set of filter specifications can be determined by automated tools [23, 24], mathematically formulated by hand or derived from a nomograph [25] defined for the specific filter. All methods yielded a minimum fifth–order requirement for this design.

The prototype LC ladder is shown is Figure 4. The normalized element values are derived using filtorX, an interactive filter design program [23]. Given a filter's performance specifications, filtorX creates the filter's transfer function. Synthesis of a lossless ladder filter is performed using the pole removal method on an impedance function obtained from the transfer function.

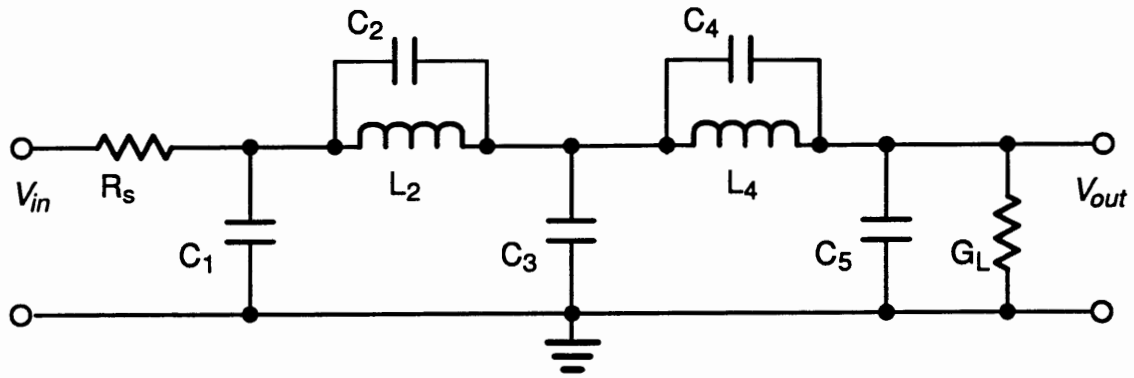


Figure 4. Prototype LC ladder structure

The normalized transfer function of poles and zeros from filtorX simulation is shown in Table I

TABLE I FILTORX GENERATED NORMALIZED TRANSFER FUNCTION ROOTS

gainCoefficient:	0.02768998047
Zeros:	0 – 3.402603233j
	0 + 3.402603233j
	0 – 2.102924448j
	0 + 2.102924448j
	0.0 – Infinityj
Poles:	–1.155332927
	–0.838063609 + 0.7031805703j
	–0.838063609 – 0.7031805703j
	–0.274242136 + 0.9747359474j
	–0.274242136 – 0.9747359474j

The normalized ladder elements for a fifth–order, inverse Chebyshev filter are listed in Table II. Determining final values for ladder elements, C_i, C_{Li}, R_s, and G_L, is a matter of scaling with the relationships,

The normalized ladder elements for a fifth–order, inverse Chebyshev filter are listed in Table II. Determining final values for ladder elements, C_i, C_{Li}, R_s, and G_L, is a matter of scaling with the relationships,

$$C_i = n_{ci} \cdot \frac{g_m}{\omega_n} \ , \quad C_{Li} = n_{Li} \cdot \frac{g_m}{\omega_n} \ , \quad R_s = \frac{1}{g_m} \ , \quad G_L = g_m \ .$$

TABLE II NORMALIZED LC LADDER VALUES

REFERENCE	NORMALIZED VALUE
R_s	1.0000000000000000e+00
C_1	4.3485318267315393e–01
L_2	1.3224013330698863e+00
C_2	1.7099735053346174e–01
C_3	1.8241330933041475e+00
L_4	1.4645551274068236e+00
C_4	5.8975503268398961e–02
C_5	5.4198694904574174e–01
G_L	1.0135361094696607e+00

The resulting normalized frequency responses of this fifth–order, inverse Chebyshev filter are shown in the following figures. Figure 5 shows the magnitude in dB of $H(j\omega_n)$. The normalized phase response $\phi(\omega_n)$ is shown in Figure 6. The 360° phase shifts are due to the range of arctangent function and are not actual frequency response variations.

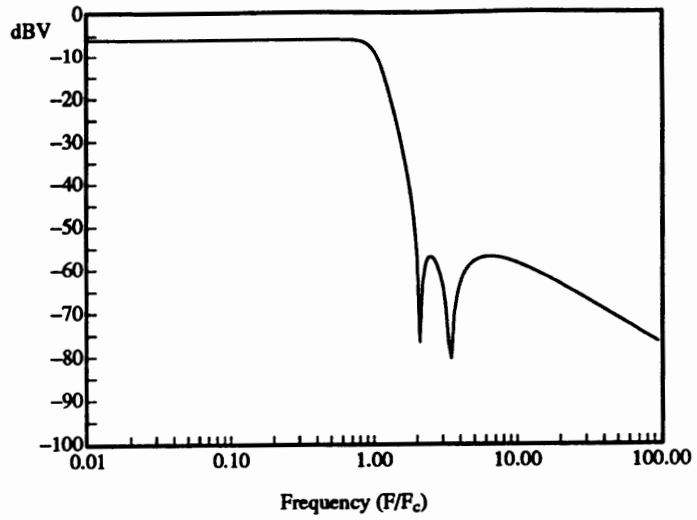


Figure 5. Prototype fifth–order inverse Chebyshev LC ladder magnitude response

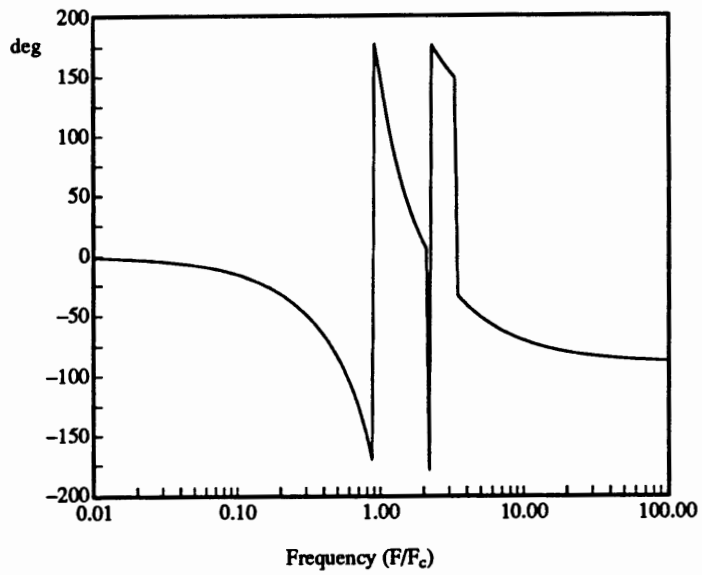


Figure 6. Prototype fifth–order inverse Chebyshev LC ladder phase response

The group or envelope delay, $\tau(\omega_n)$, is another important filter response. The filter gain response may be defined as

$$H(j\omega) = |H(j\omega)|\, e^{j\phi(\omega)}$$

where $\phi(\omega)$ is the phase. The group delay is defined as the negative of the derivative of the phase with respect to frequency [26] ,

$$\tau(\omega) = -\frac{d\phi}{d\omega} \quad .$$

The normalized delay response for this prototype filter is shown in Figure 7.

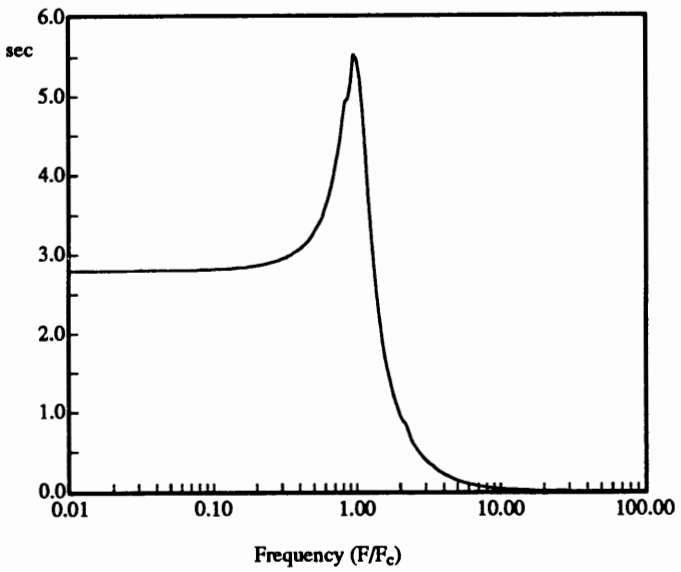
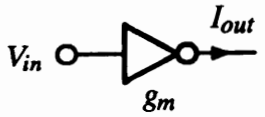


Figure 7. Prototype fifth–order inverse Chebyshev LC ladder group delay response

Concepts for Automated Filter Design

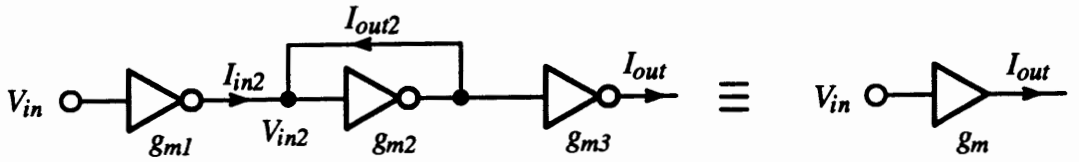
The active LC ladder filter is chosen for this project primarily in response to automated filter realization concerns [27]. It has been shown that transconductor–grounded capacitor (TGC) filters can be generated by signal–flow–graph methods for VLSI implementation [28, 29]. This representation illustrates that an LC ladder filter can be simulated by only series admittance arms, Y_i , combined with shunted impedance arms, Z_i . The recursive properties of the resulting continuous fraction readily applies itself to design automation. An expansion of the fraction reveals that repeated operations of addition and inversion of immittance values are all that is required [18]. This method requires only transconductors and capacitors for LC ladder simulation. For this single–ended design with transmission zeros, floating capacitors are also necessary. Design is performed using normalized values for frequency and transconductance which are then scaled depending on circuit specifications.

Representation of the simulated ladder topology with only admittance and impedance branches requires a minimum of building blocks. The active filter realized here uses only capacitors and g_m cells of *identical* value. There are two basic building blocks in this design. The circuit symbol for the inverting transconductance element is shown in Figure 8, and the noninverting transconductance element is shown Figure 9 [28].



$$F(s) = I_{out} = -g_m \cdot V_{in}$$

Figure 8. Inverting transconductance circuit symbol



$$F(s) = I_{out} = g_m \cdot V_{in}$$

Figure 9. Noninverting transconductance circuit symbol

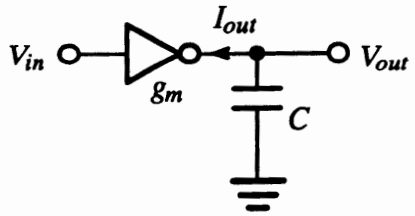
The required functions are easily implemented using these current mode devices with grounded capacitors. A simple derivation shows that the configuration of the second cell in Figure 9 is equivalent to a grounded resistor, where,

$$I_{in2} = -I_{out2} \quad ,$$

and

$$\frac{V_{in2}}{I_{in2}} = R_{in2} = \frac{1}{g_{m2}} \quad .$$

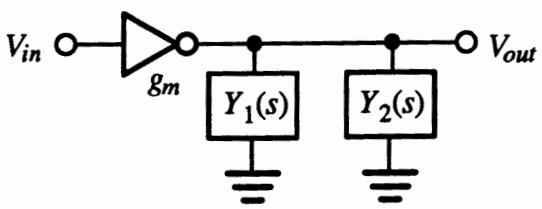
It is also apparent that if the first two cells have equal g_m values then they function as a unity gain buffer. The integration function is created using a g_m cell loaded by a grounded capacitor, as realized by the configuration in Figure 10.



$$F(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m}{sC}$$

Figure 10. Integrator circuit symbol

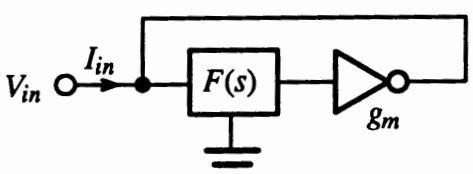
The addition and inversion of more than one admittance is accomplished by the circuit shown in Figure 11.



$$F(s) = \frac{V_{out}}{V_{in}} = -\frac{g_m}{Y_1(s) + Y_2(s)}$$

Figure 11. Addition and inversion circuit symbol for voltage transfer function

And finally, the inversion of the voltage transfer function back into an admittance is accomplished by the circuit in Figure 12.



$$Y(s) = \frac{I_{in}}{V_{in}} = g_m \cdot F(s)$$

Figure 12. Inversion circuit symbol for admittance realization

The fifth–order inverse Chebyshev active ladder topology in g_m–C form is shown in Figure 13.

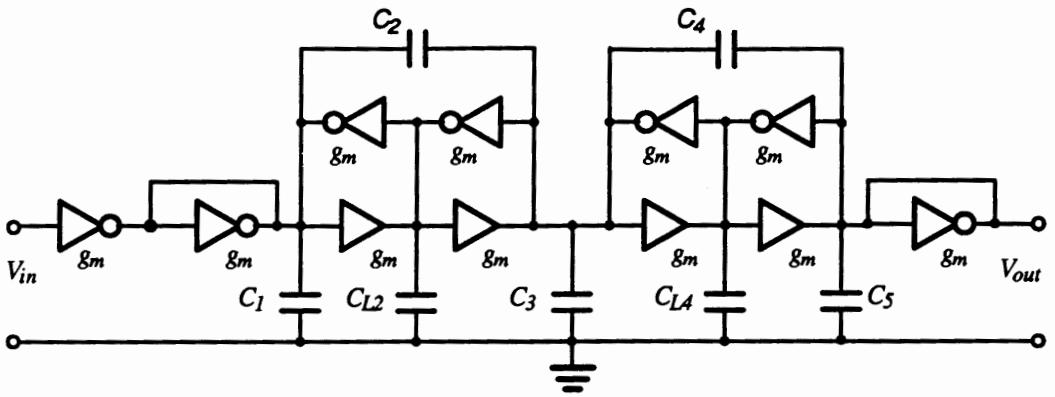


Figure 13. Fifth–order inverse Chebyshev filter

The first cell converts the input voltage, V_{in} , to a current, the second cell is the grounded source resistance and the final cell is the load element for V_{out} . Using the SFG method, and neglecting source and load elements, the input admittance, $Y(s)$, of the transfer function, $H(s)$, is expressed by the continuous fraction:

$$Y(s) = sC_1 + \cfrac{g_m^2}{\cfrac{g_m^2}{sC_2 + \cfrac{g_m^2}{sC_{L2}}} + \cfrac{g_m^2}{sC_3 + \cfrac{g_m^2}{\cfrac{g_m^2}{sC_4 + \cfrac{g_m^2}{sC_{L4}}} + \cfrac{g_m^2}{sC_5}}}}$$

An important feature of this filter topology is that almost all of the inherent MOS input and output capacitors are shunted by grounded circuit capacitors. This relationship allows these pesky parasitics to be absorbed into the design. This effectively limits the undesirable effects of these parasitics in all but the non–inverting transconductance element. Referring back to Figure 9, it is apparent that there is a hidden internal node, V_{in2} , which is inaccessible for absorption.

Gm–C Filter Layout

Transconductance cells are laid out for fabrication using Magic. This program uses the "lambda" based design rule of Mead and Conway. Consideration of the influences of capacitive and resistive interconnect dominate cell layout and signal routing. The signal path from input to output is kept as short as possible and symmetry between the transistor pairs is maintained for best possible device matching. To prevent against latchup, ohmic contacts are placed on the negative supply rail and n–diffusion guard rings enclose the n–wells. Bias voltages or control lines are run in metal2 horizontal to the cell. The analog signal path runs in metal2 vertical to the cell. To facilitate the automated filter realization process, four cells are created for final assembly of the filter. A non–inverting and inverting cell in the forward direction and a noninverting and inverting cell in the backward direction. Layout paint geometry for the noninverting and inverting cells are shown in Appendix C on pages 86 and 87.

Final layout of the filter is performed using an automated analog filter design tool currently being developed [13]. The capacitor grids are an integral part of the automated filter layout tool and minimal adjustments in dimensions specific to this filter are performed. Predistortion is performed to include the inherent C_i and C_o of the g_m cells and interconnect capacitors. Cells are connected by abutment, minimizing total area requirements and unpredictable parasitics. Minimal designer intervention is required in the final phases. Creation of the two series capacitors is done by hand using identically sized poly1/poly2 grid squares. The DC biasing circuitry is also routed by hand along with the final I/O routing to the pad frame. Symmetry between identical single–ended filters is

maintained in anticipation of differential operation. Final chip layout is shown in Appendix C on page 89 with the expansion of one of four filters.

SIMULATION TECHNIQUES

Transconductance Element Simulation

The AC response of a single transconductance cell depends on the applied load. It is not uncommon for one g_m cell to be loaded by one or more g_m cells. In order to observe the behavior of an individual g_m cell, the configuration previously described as the negative unity gain buffer is employed. This test structure is shown in Figure 14. The I_{test} ammeter is inserted in the simulation deck only. Testing is performed on the extracted layout to measure dynamic range of operation, frequency magnitude and phase/delay response.

Dynamic range of operation is determined primarily by the the threshold voltages of the devices and can be expected to be approximately $2 \cdot V_t$. This comes from the fact that devices are operated in saturation which implies,

$$-|V_{tp2}| < V_{in} - V_{out} < V_{tn3} \ .$$

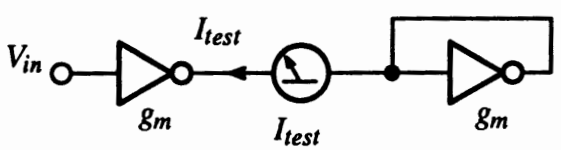


Figure 14. Loaded transconductance test circuit symbol

A DC voltage is applied to the input and varied from –2V to +2V. An important observation in this experiment is the zero–in, zero–out crossing. Failure to meet this common behavior of a lossless, twoport structure implies a

DC offset at the output and the potential for signal distortion. It is assumed from earlier mathematical derivations that body effects are cancelled by total symmetry. However, unless a twin–tub process is available, it is not possible to tie all of the device sources to the bulk. This circuit configuration did observably suffer from the non–cancellation of V_{BS} in M2 and M4 and was nullified directly. DC response for an average model and aspect ratio is shown in Figure 15.

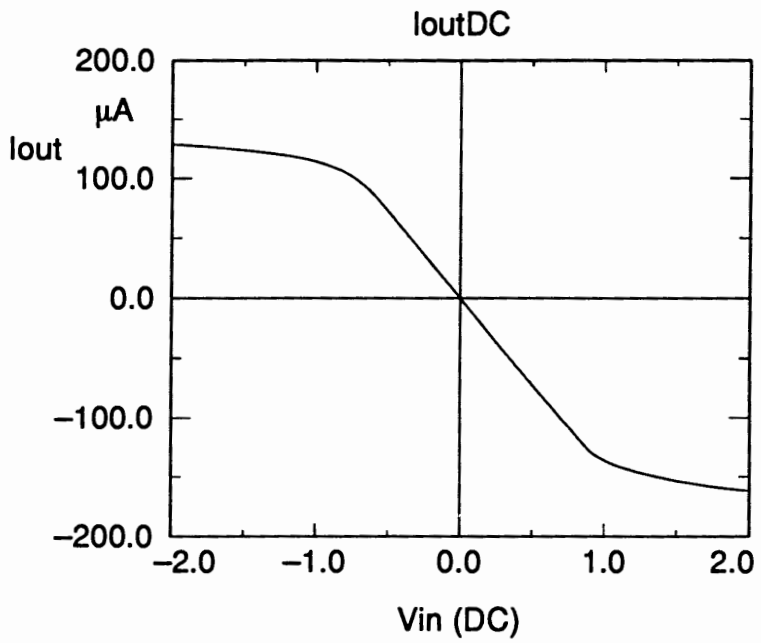


Figure 15. Gm cell simulated DC output current

The transconductance gain of the cell is a measure of the change in output current to a change in the input voltage, V_{in}. This is obtained by taking the derivative of the current I_{test} with respect to the input voltage. A constant value of this derivative is most desirable. The gain level is variable by adjusting the bias voltage V_{G1} and V_{G4}. The measurement for this g_m cell is shown in Figure 16.

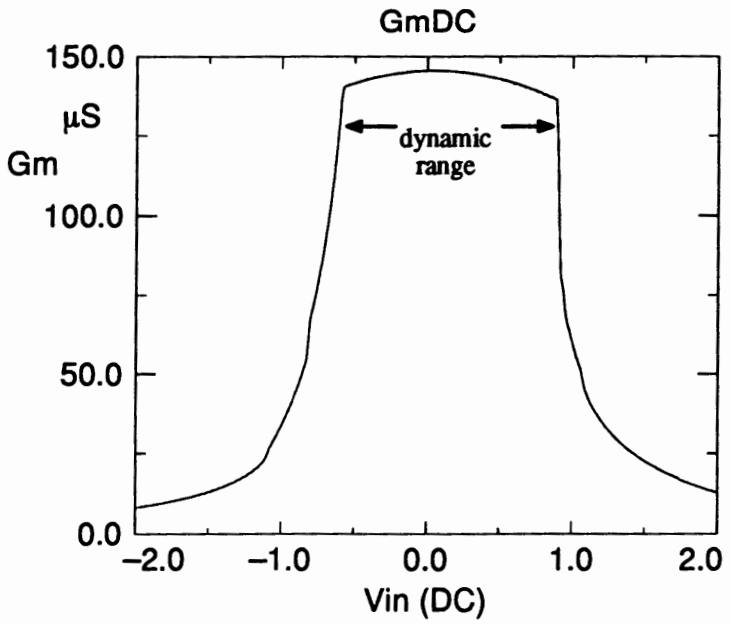


Figure 16. Gm cell simulated transconductance

The AC response of the individual cell is also indicative of the final filter performance. This response is computed by applying a sweep of sinusoidal signal frequencies at a constant magnitude to the test circuit. For this device, a 1V peak to peak signal is applied, and frequency is varied from 100kHz to 100GHz. Bandwidth at the –3dB point is defined as the cutoff frequency range, or half–power point. A filter's characteristic operating frequency is designed to well below the bandwidth of the transconductor. This simulated AC magnitude response is shown in Figure 17.

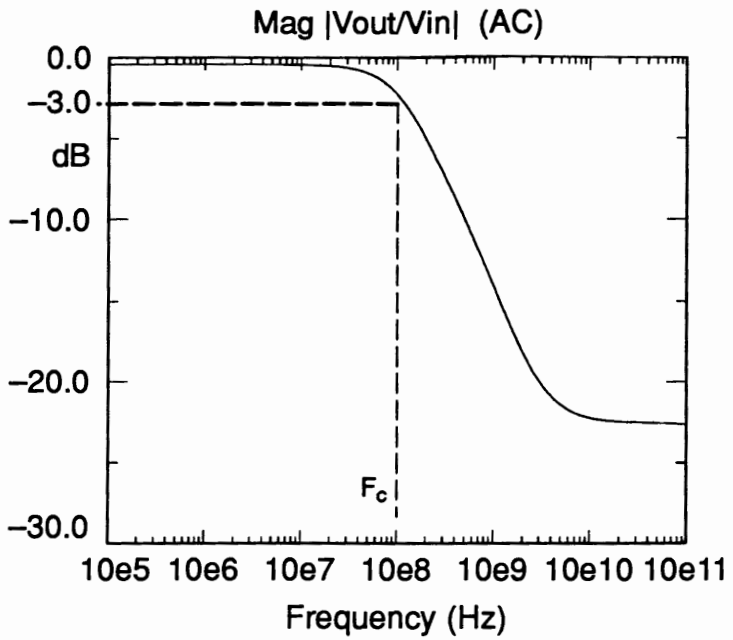


Figure 17. g_m cell simulated AC magnitude response

Ideally, at low frequency, there should be a unity gain response. The nonzero output, (–0.4dB), is due to the non–ideal output characteristics of the device. There is finite output conductance, g_o , in parallel with the ideal current source which creates this DC loss.

The group delay response of the test circuit is shown in Figure 18. Again, it is the flatness of waveform or a constant phase change with respect to a changing frequency that is desirable within the bandwidth of the transconductance cell.

A sample of SPICE simulation code is supplied in Appendix B on page 81. This code is used for simulation of the transconductance cell DC and small–signal responses.

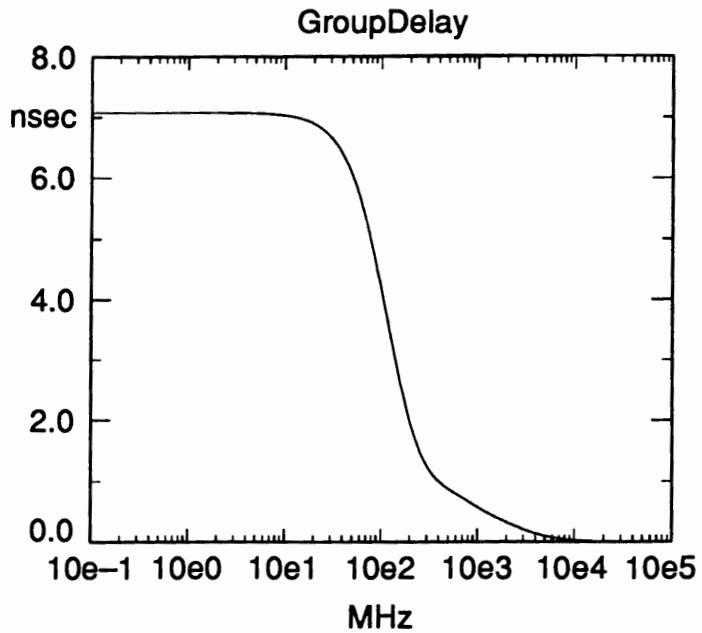


Figure 18. Gm cell simulated group delay

Input and Output Capacitor Values

An important variable in the performance of the high–frequency filter is the input and output capacitance of the transconductance cell. The ability to predistort the final design capacitors to incorporate these parasitic capacitors requires accurate values for each of these parasitics. Layout extraction can provide good estimates of C_i and C_o. However, extracted values are better approximations when the transconductance cell has large C_i and C_o. For the simple single–ended cell used in this experiment, the extracted values for C_i and C_o are small, 5fF and 61fF respectively, and additional small–signal simulations are required to refine these estimates.

The analysis of the small–signal performance of an MOS transistor is a complex and difficult problem. It has been demonstrated [5], that the MOS transistor can be modeled as in Figure 19.

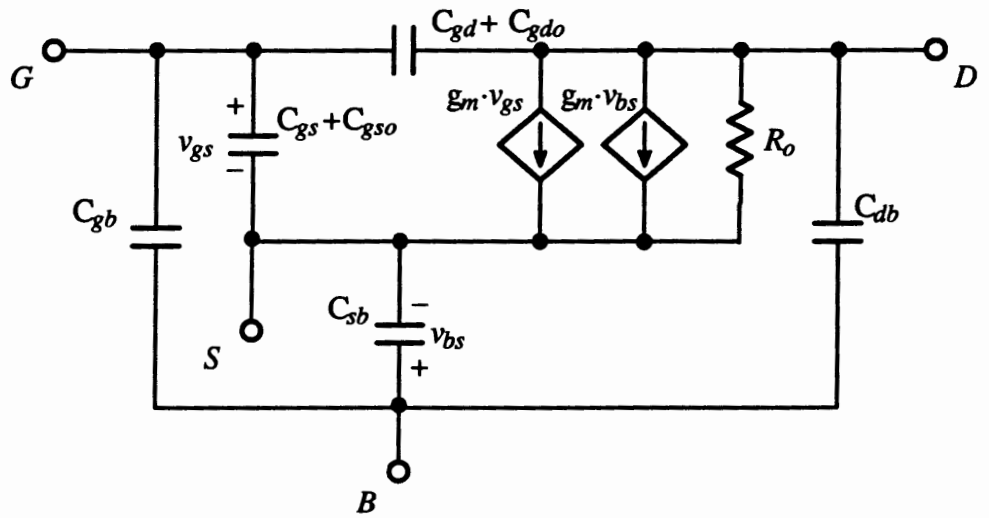


Figure 19. Complete MOSFET small–signal equivalent circuit model

Inherent MOSFET parasitic capacitors, in addition to being numerous, are further complicated by voltage dependencies. Recalling that the transistors used in the transconductance cell are arranged in a composite configuration, further complicates the numerical analysis. Fortunately, discrete capacitor values for each parasitic are not required and the total input capacitance value and the total output capacitance value are sufficient enough for the predistortion procedure employed here.

Simulation is performed to determine the inherent MOS input and output capacitance of the transconductance amplifier depicted by a simplified small–signal model in Figure 20. The simple method to measure the

small–signal capacitance values of a transconductor can be explained as follows:

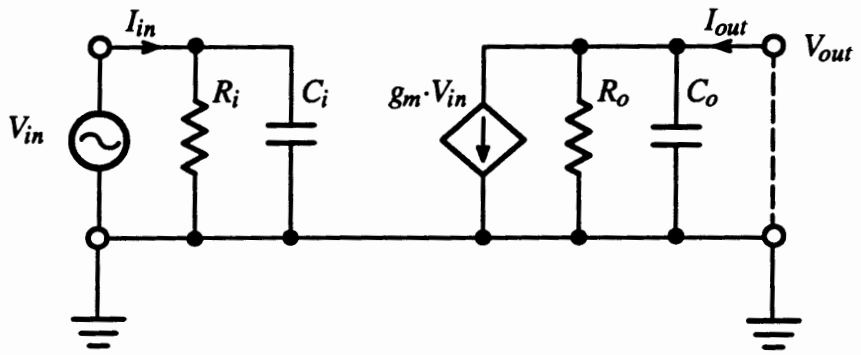


Figure 20. Simplified small–signal inverting transconductance model

At DC a capacitor behaves as an open circuit, and the impedance of a circuit is determined by R. At higher frequencies however, the capacitor is the dominant impedance element. For C_i, V_{out} is grounded and the current I_{in} is measured. In the same manner for C_o, V_{in} is grounded and the current I_{out} is measured. Utilizing the simple equation for capacitor current, $i_c \cdot dt = C \cdot dv_c$ and solving for C, values are derived for both the input and the output capacitors for the cell. Results are shown in Table III by MOSIS process run. Extreme value runs are shaded. Note that the parasitic input capacitance derived by simulation is approximately seven times as large as the layout extracted value. The parasitic output capacitor derived by simulation is closer to the extracted value, varying only by about 15%.

TABLE III SIMULATED INPUT AND OUTPUT CAPACITANCE

RUN ID	N3AB	N38L	N37C	N34O	N32A	N2CQ	N2BE	N25Y
C_i (fF)	33	36	36	33	35	38	34	32
C_o (fF)	71	75	75	70	72	77	72	70

	Mean	MIN	MAX	% Δ	STD	% Δ_{STD}
C_i (fF)	34.6	32	38	15.8	1.9	5.5
C_o (fF)	72.8	70	77	9.1	2.5	3.4

Filter Simulation

In the g_m-C continuous–time filter there are two elements which affect overall filter performance; poly1/poly2 capacitor and the MOSFET gain cell, g_m. Both elements are dependent on process variations and therefore both variables are investigated. The frequency, gain, and capacitor relationship in a g_m-C filter is shown in the equation,

$$\omega = \frac{g_m}{C} \quad .$$

Given this equation, it is expected that filter performance is dependent on process parameter variations. Recall that the transconductor gain is dependent on the MOSFET model. This would imply that filter magnitude and bandwidth vary with process parameter variations. The final grounded capacitor value is a combination of the circuit poly1/poly2 capacitor tiles and the MOSFET parasitic capacitors. The capacitor value is therefore dependent on both the poly1/poly2 and the MOSFET process dependent parameters. This would imply that the filter performance is also dependent on both the process variable capacitance and the MOSFET process dependent parameters.

Simulation experiments are performed on three arrangements of filter element models:

a. Variable MOSFET models with a fixed capacitance unit value,

b. Average MOSFET model with variable run capacitance unit values, and,

c. Process run MOSFET models with same run capacitance unit value.

To evaluate the three distinct element couplings without introducing new variables, nominal control voltages are applied to the test figure, and no g_m tuning is performed. Tests are performed using the same input signal and sweep range. Primary responses investigated are high–frequency magnitude, phase and group delay.

Figure 43, in Appendix C on page 88, shows a typical Magic layout for a grounded capacitor including interconnect. Note that the two rightmost grid squares are empty. The capacitance values for poly1/poly2 are listed in Table IV by MOSIS process run. Actual tile size used in filter fabrication is 12 μm x 9 μm, or 108 μm^2. Extreme value runs are shaded.

TABLE IV POLY1/POLY2 CAPACITANCE

RUN ID	N3AB	N38L	N37C	N34O	N32A	N2CQ	N2BE	N25Y
fF/μm^2	0.459	0.481	0.463	0.470	0.456	0.469	0.447	0.480
fF/Tile	49.572	51.948	50.004	50.760	49.246	50.652	48.276	51.840

	Mean	MIN	MAX	% Δ	STD	$\%\Delta_{STD}$
fF/μm^2	0.4656	0.447	0.481	7.07	.012	2.58
fF/Tile	50.288	48.276	51.948		1.27	

The first simulation set varies the MOSFET model with a fixed value of the unit capacitor. The value of poly1/poly2 used is 0.474fF/μm^2. This value yields approximately a 52.488fF grid square capacitance and is the capacitance value used during the automated filter synthesis.

The second set simulates a fixed MOSFET model with a varying value of the poly1/poly2 unit capacitance. Preliminary testing of the transconductance cell and overall filter performance reveals that process run N38L provides average filter response characteristics. Unit capacitance per grid square is varied in the simulation deck The capacitor tile size is maintained constant but the resulting capacitance value is a variable.

The third and final simulation set varies the MOSFET model simultaneously with the same process run value of poly1/poly2 capacitor. Unit capacitance per grid square is varied in the simulation deck with the MOSFET device model. The capacitor tile size is maintained constant but the resulting capacitance value is a variable.

CHAPTER III

FINDINGS

OVERVIEW

This chapter presents SPICE (Simulation Program with Integrated Circuit Emphasis) simulation results. The analysis of process dependence is performed on the layout extracted low–pass, fifth–order, inverse Chebyshev, g_m–C filter design. Interval levels of measurement record the quantitative data in a tabular format, whereas response plots create valuable graphical representation. The response characteristics of the tested device models are organized as a basis for a system of classification. A representation of an ideal, prototype LC ladder filter is included for comparison where applicable. Deviations from ideal filter characteristic behavior is analyzed and cause of the deviations are related to the normal process variation of the 2μm process investigated.

SIMULATION FINDINGS

MOS Model Selection

As the investigation of process dependence continues, it is determined that four models (33% of total available) are not acceptable. These models are deemed unacceptable due to misleading representation of minimum sized device threshold voltages. As sizes are increased, representation of the device does approach expected values. It is possible that the cause of these discrepancies is due to inaccurate junction capacitance value. It is important to note that the MOSIS provided SPICE model parameters (Level 2) are obtained by transistor level DC curve fitting methods. A parameter optimizer measures the I–V data from fabricated transistors to obtain the SPICE model parameters. The resulting SPICE parameters are used to simulate a set of inverters and a ring oscillator. Differentially based, small–signal parameter values can be far from their actual value. For this study, emphasis is placed on the ability to accurately predict high–level circuit tracking of process dependent models.

Filter Specifications Investigated

As explained earlier, deviation from the ideal amplitude or phase characteristics across the frequency band of interest must be kept at a minimum in order to obtain a good quality analog signal transmission or low error performance of data transmission. Unexpected output may be caused by signal crosstalk, echoes, nonlinear behavior of active devices, coupled noise, and random noise from a variety of sources. One benefit of this simple transconductance design and filters composed of this transconductance cell is the relatively low number of active devices. This reduces the occurrences of

shot noise generated by gate leakage currents and larger scale thermal noise contributions. The group delay performance, also reflected by the phase response, is another important characteristic. High–Q filters that generate narrow transition bands show a higher delay peaking value than the maximally flat filter of the same order. The delay should be constant. When phase has a linear dependence on frequency, the group delay will be constant and filter exhibits no phase distortion. In a maximally flat filter, it is expected that the delay is greatest at the passband edge. This is where the dominant poles take effect and phase change is greatest with respect to a small change in frequency. For designs with a positive Q, attenuation increases with the same frequency dependence as delay [18]. Therefore, in active LC ladder structures, errors in attenuation occur at the passband edge, as observed by the gain 'bump'.

Knowing which aberrations in signal response to expect provides additional insight as to which important filter behavior to investigate. The design characteristics for this fifth–order inverse Chebyshev are shown in Figure 2 on page 8. This study of active filter performance will concentrate on how these magnitude and phase/delay characteristics relate to variations of process parameters. The minimum and maximum frequency response variations for each simulation set is identified by its process run label. These process runs form the *envelope,* (ENV), of response spread extremes. The LC ladder prototype behavior is labeled PROTO.

Filter Performance Findings

Recall from the previous chapter that three sets of simulation are performed on the g_m–C filter. The results from simulation involving the variation of the MOSFET model with a fixed poly1/poly2 capacitance value are listed in Table V and shown in Figures 21, 22, and 23,

TABLE V FILTER RESPONSE FOR VARIABLE MOSFET MODEL, FIXED POLY1/POLY2 CAPACITANCE

RUN ID	DC –dB	F_c @ –3dB MHz	F_s 36MHz –dB	F_c 18MHz –dB	GrpDel Max MHz
PROTO	6.00	18.00	59.09	9.18	17.38
N3AB	7.90	16.15	52.66	17.37	15.14
N38L	8.20	21.32	43.77	7.70	19.95
N37C	8.43	22.90	39.59	7.89	21.88
N34O	7.91	18.36	49.74	10.69	17.38
N32A	7.95	18.36	49.40	10.23	17.38
N2CQ	8.42	22.24	41.35	7.79	20.89
N2BE	8.06	17.60	50.94	13.01	16.60
N25Y	7.94	20.04	46.85	8.22	19.05
ENV H	8.43	22.90	39.59	7.70	21.88
ENV L	7.90	16.15	52.66	17.37	15.14
Δ ENV	0.52	6.75	13.07	9.67	6.74

The envelope of response is bounded by device models N3AB and N37C. Response crossing at the transition band frequency is due to Q enhancement behavior only. Spread of filter specification is 6.75MHz at the passband edge, with three tested models, (37.5%), within 500kHz of target cutoff frequency. The phase envelope is bounded by the same two models, as is the group delay response.

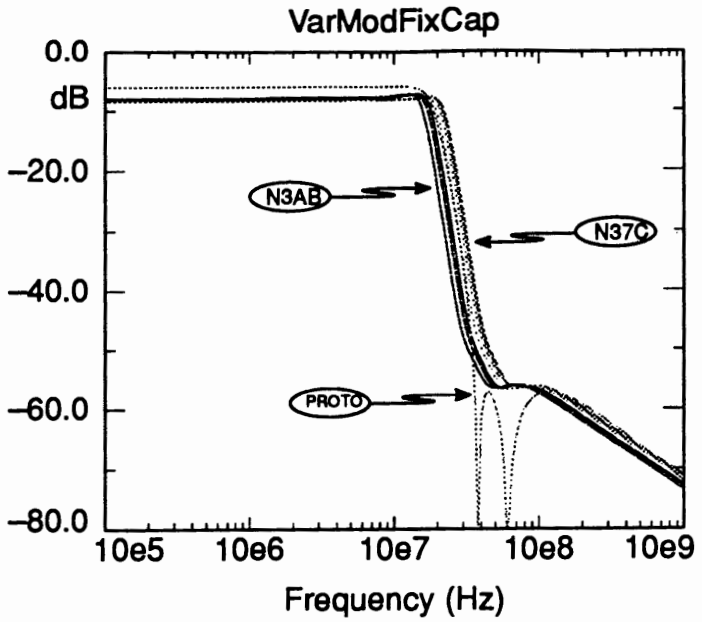


Figure 21. Magnitude response variable MOSFET model with fixed poly1/poly2

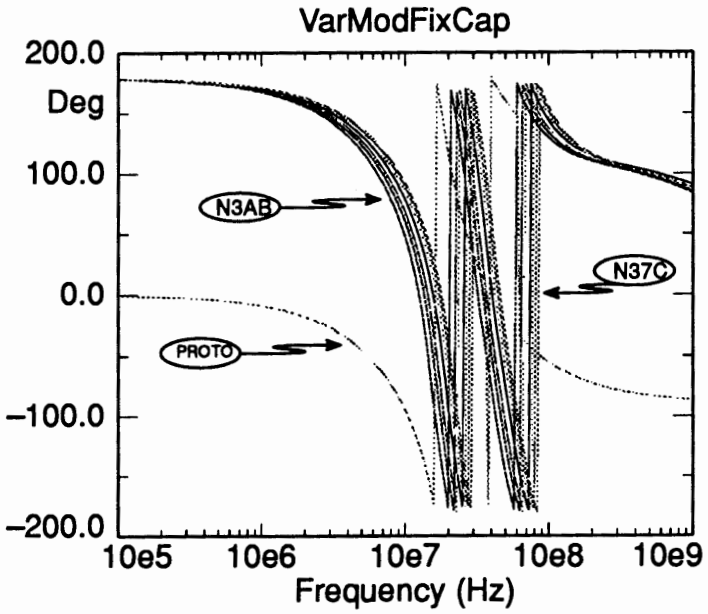


Figure 22. Phase response variable MOSFET model with fixed poly1/poly2

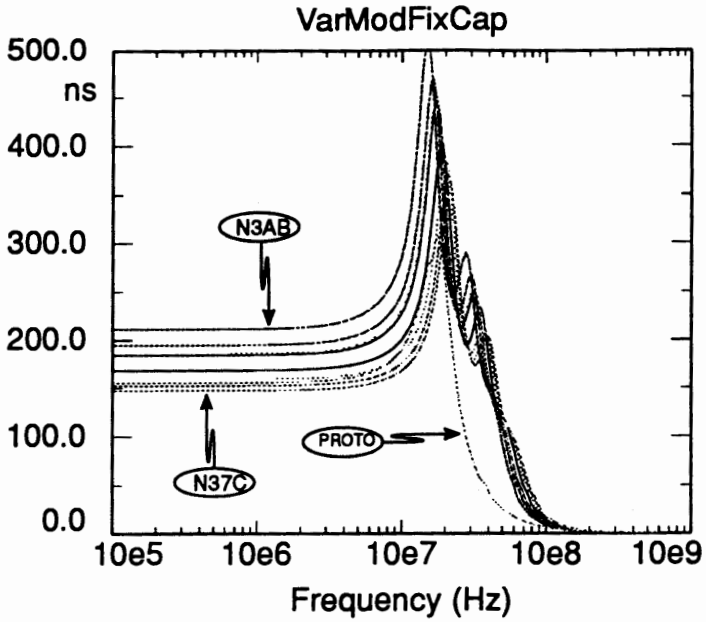


Figure 23. Group delay response variable MOSFET model with fixed poly1/poly2

Simulation results reveal a smaller spread of values for filter response with respect to capacitor poly1/poly2 variation. In the previous chapter, it was determined that the variation of the poly1/poly2 capacitance is relatively small. Table IV on page 34 shows approximately a 1.25fF standard deviation per capacitor grid tile. For the largest capacitor in this design, that amounts to a mere 47.5fF, or less than one tile. This is comparable to a rounding error in the automated design routine, as capacitor grid units are integers. Component values used in the fifth–order inverse Chebyshev active LC ladder filter shown in Figure 13 are listed in TABLE VI.

The simulation results for the fixed MOSFET device model with a variable poly1/poly2 capacitance value are listed in TABLE VII and shown in Figures 24, 25, and 26.

TABLE VI FIFTH–ORDER INVERSE CHEBYSHEV ACTIVE LC LADDER FILTER VALUES

REFERENCE	SCALED COMPONENT VALUES
R_s	6.67kΩ
C_1	353fF
CL_2	1.52pF
C_2	227fF
C_3	2.196fF
CL_4	1.72pF
C_4	78fF
C_5	495fF
$G_L=1/R_s$	150μS

TABLE VII FILTER RESPONSE FOR FIXED MOSFET MODEL, VARIABLE POLY1/POLY2 CAPACITANCE

RUN ID P1/P2	DC –dB	F_c @ –3dB MHz	F_s 36MHz –dB	F_c 18MHz –dB	GrpDel Max MHz
PROTO	6.00	18.00	59.09	9.18	17.40
N3AB	8.20	21.46	43.77	7.70	19.95
N38L	8.20	21.60	43.30	7.63	19.95
N37C	8.20	22.21	41.52	7.47	20.89
N34O	8.20	22.21	42.23	7.52	20.89
N32A	8.20	22.56	40.78	7.42	21.00
N2CQ	8.20	22.02	42.13	7.51	20.40
N2BE	8.20	23.01	39.81	7.39	21.50
N25Y	8.20	21.60	43.21	7.62	19.95
ENV H	8.20	23.01	39.81	7.39	21.50
ENV L	8.20	21.46	43.77	7.70	19.95
Δ ENV	0.00	1.55	3.96	0.31	1.55

The envelope of response is defined by model N3AB and N2BE and is 77% narrower in frequency range than the first simulation set. Model N2BE does have the minimum value of poly1/poly2 capacitance, however, model N3AB does not have the maximum value.

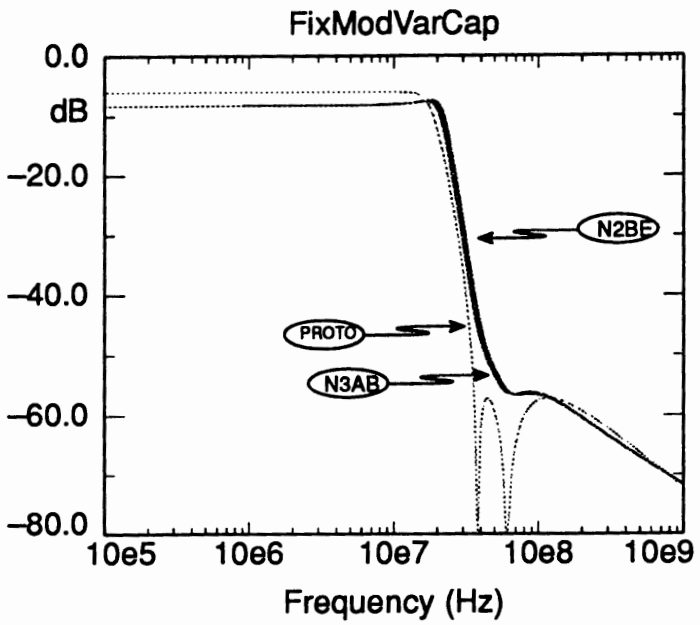


Figure 24. Magnitude response for fixed MOSFET model, variable poly1/poly2

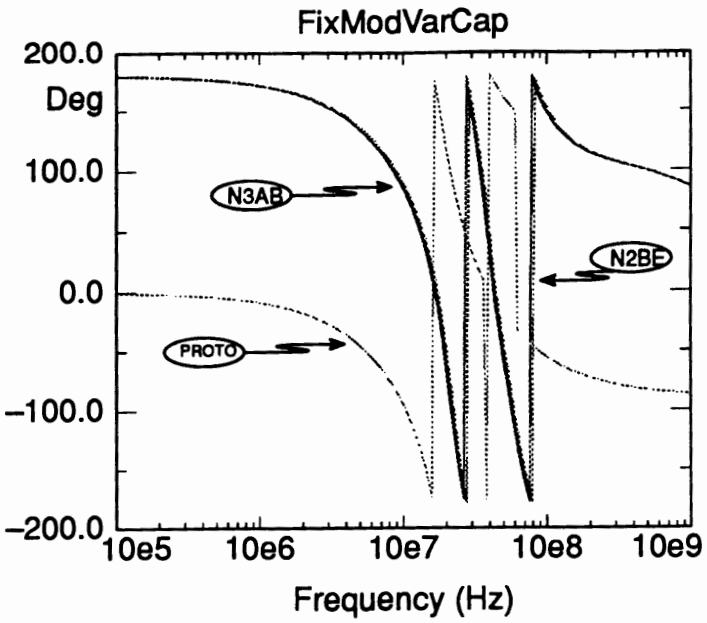


Figure 25. Phase response for fixed MOSFET model, variable poly1/poly2

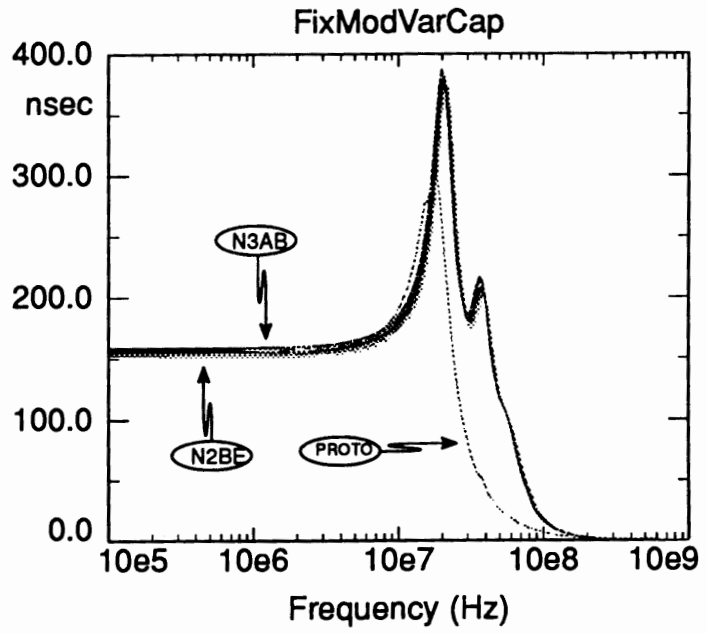


Figure 26. Group delay response for fixed MOSFET model, variable poly1/poly2

The final simulation set investigates the performance characteristics of the filter with the process run MOSFET model and its measured run poly1/poly2 capacitance value. It is not surprising that these results would parallel the first set as the capacitance variation effect was shown to be minimal for this filter. A uniform shift towards a higher passband edge is caused by the lower unit capacitance values of poly1/poly2 than that used in the first simulation set. The results from the third set of simulation are listed in TABLE VIII and shown in Figures 27, 28, and 29.

TABLE VIII FILTER RESPONSE FOR VARIABLE MOSFET MODEL, VARIABLE POLY1/POLY2 CAPACITANCE

RUN ID	DC –dB	F_c @ –3dB MHz	F_s 36MHz –dB	F_c 18MHz –dB	GrpDel Max MHz
PROTO	6.00	18.00	59.09	9.18	17.38
N3AB	7.90	16.86	51.70	14.60	15.85
N38L	8.20	21.60	43.30	7.63	19.95
N37C	8.43	37.06	37.06	7.80	22.43
N34O	7.91	18.85	48.99	9.60	17.38
N32A	7.95	19.54	47.80	8.46	18.20
N2CQ	8.42	23.10	39.59	7.70	21.39
N2BE	8.06	18.90	49.25	9.89	17.38
N25Y	7.94	20.31	46.40	8.03	19.05
ENV H	8.43	24.02	37.06	7.63	22.43
ENV L	7.90	16.86	51.70	14.60	15.85
Δ ENV	0.53	7.16	14.64	6.97	6.58

The response envelope is bounded by process runs N3AB and N37C, as in the first set. Spread of filter passband specification is 7.16MHz The phase envelope is defined by the same two models, as is the group delay.

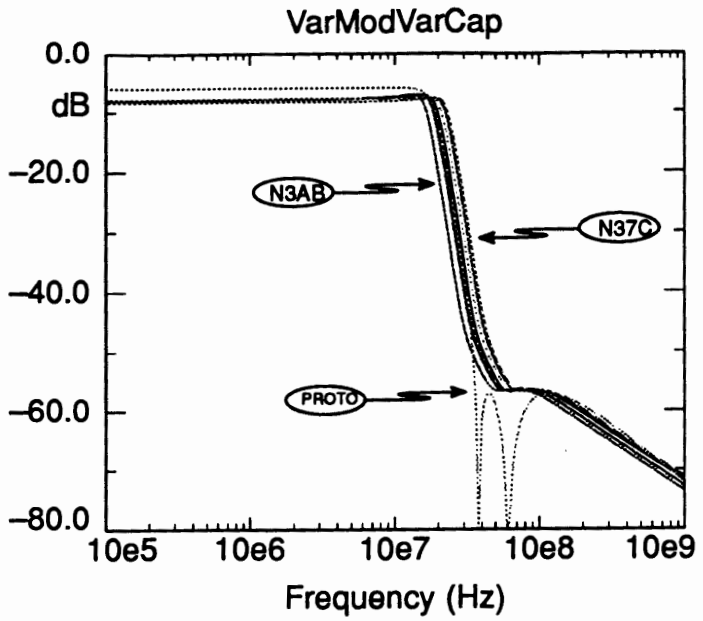


Figure 27. Magnitude response variable MOSFET model with variable poly1/poly2

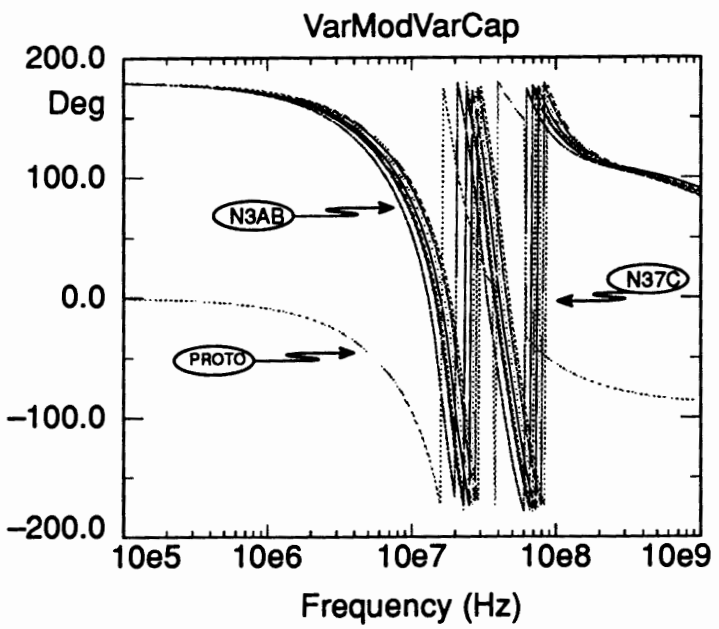


Figure 28. Phase response variable MOSFET model with variable poly1/poly2

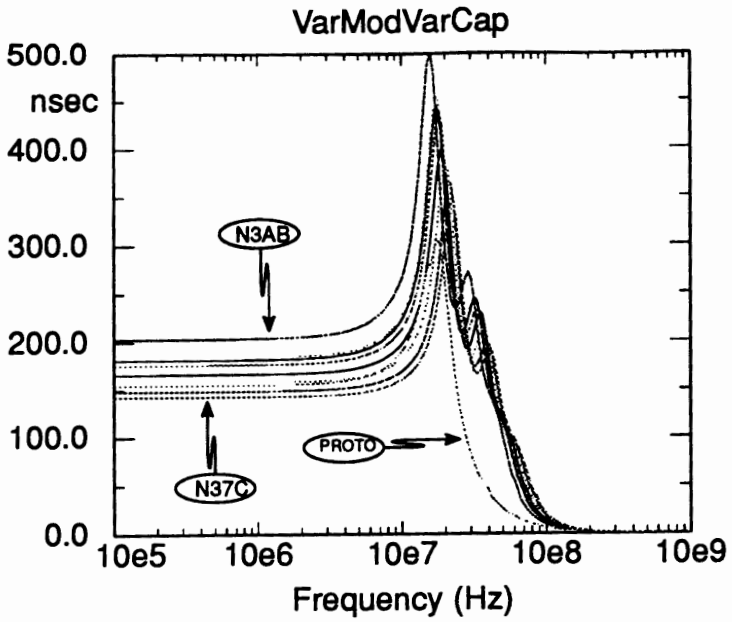


Figure 29. Group delay response variable MOSFET model with variable poly1/poly2

Explanation of Deviant Filter Behavior

The shift in frequency of the passband edge is because of the change in g_m/C ratio. Although not utilized in this study, this filter structure does have the ability to vary or electronically tune the g_m gain. Therefore, the shift is not considered to be a distortion of signal response. It is accepted that process parameter variations are unavoidable with current fabrication technology. All filters tested in this research were experimentally tuned and spanned the frequency range caused by device variations with an additional applied bias voltage of $\leqslant \pm 0.5$V. In this design, the nominal applied bias voltage is 4.0V.

The region where the distortion is largest is in the transition band. The source of the transition band distortion is the internal node capacitance of the non–inverting transconductance cell. This capacitor creates an additional pole which detrimentally influences the filter's transfer function. There is no way to absorb this capacitance as with the ability to absorb the other input and output parasitic capacitors by predistortion. However, another method of predistortion was attempted. It was observed in preliminary simulations that the effect of these parasitics not only affected the Q of the filter, thus creating the bump at the transition band, but also that the slope of the transition decreased, pulling up or decreasing the stopband attenuation at ω_s. This may be attributed to the lose of transmission zero notch depth. In order to compensate for this effect, a filter's specification of stopband attenuation can be increased or pre–emphasized. Pre–emphasis of stopband attenuation is designed into this filter. Attenuation of the filter stopband is met, although the stopband frequency of the prototype had to be increased also to maintain filter order. Although present in all simulation sets, the changes in the magnitude response transition band is most clearly observable in Figure 24.

Another anomaly in signal response is the additional loss in DC level. It was noted in the transconductance cell design section that there is a finite output conductance, g_o, as well as a finite output capacitance, C_o, in parallel with the ideal current source output of the cell. Figure 30 shows a two g_m cell circuit and a simplified, single g_m cell AC equivalent model.

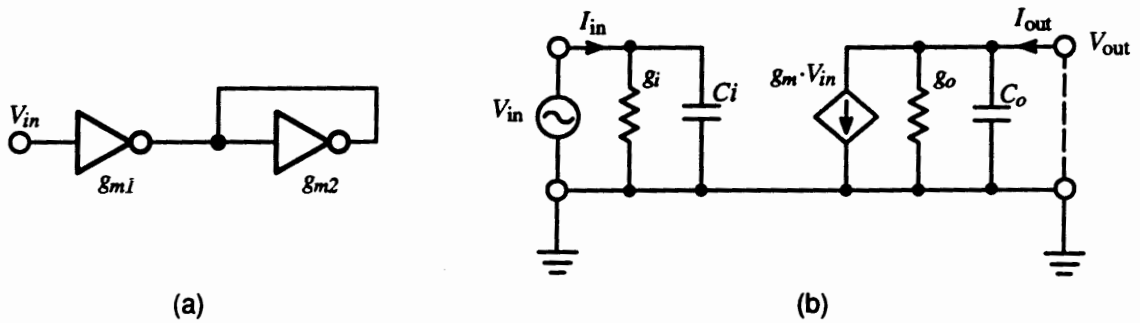


Figure 30. Transconductance cell: (a) actively loaded circuit symbol, (b) simplified, single g_m cell AC equivalent model

The DC deviation from 0dB is caused by the real part, or the inclusion of g_o in the equations. Thus, instead of having

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{m2}} \quad ,$$

which, with identical gain, $g_{m1} = g_{m2}$, would result in a unity gain, or 0dB; g_o is included which yields,

$$\frac{V_{out}}{V_{in}} = -\frac{g_{m1}}{g_{m2} + g_{o2} + g_{o1}} \quad .$$

AC simulation of the two g_m cell test circuit resulted in a –0.40dB loss.

In active LC ladder filter simulations generated by signal flow graph methods, the nodal equations of the passive LC prototype are obtained using

inverting and non–integrators [32]. If all of the parasitic admittance is included in the transfer function equation of the integrator then,

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m}{sC + sC_o + g_o} \quad .$$

In addition, if the transconductance cell is loaded, as is the case of the final active filter design then the input impedance of the loading stage will also enter into the equation [18],

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m}{sC + sC_i + sC_o + g_o + g_i} \quad .$$

Considering that the MOSFET device normally has a very high input impedance, in general g_i is negligible.

The predistortion step in the design process absorb most of the input and output capacitors, however, g_o remains and it creates a lossy integrator [33], which is considered to be a main problem in the design of high–frequency, active filters [34, 35]. An ideal integrator has a finite DC gain associated with it and is represented in the *s* domain as,

$$\frac{V_{out}}{V_{in}}(s) = \frac{\omega_o}{s} \quad , \quad \omega_o = \frac{g_m}{C} \quad .$$

This implies a pole at the origin and a 90° phase shift at the unity gain frequency at $\omega = g_m / C$. With the inclusion of g_o , the integrator is defined as lossy and the transfer function can be represented by [33],

$$\frac{V_{out}}{V_{in}}(j\omega) = \frac{g_m}{j\omega C + g_o} \quad .$$

This introduces an undesirable phase shift defined by,

$$\phi' = -\arctan\left(\frac{\omega C}{g_o}\right) \approx -\frac{\omega C}{g_o} \quad .$$

In terms of delay this equation may be rewritten as [13]

$$\phi' \approx -\frac{\omega C}{g_o} \approx -\omega\tau \quad .$$

The loss of the transmission zero notch attenuation is due to these finite parasitic conductance variables. A gyrator configuration, along with the accompanying capacitors, simulates the behavior of the LC tank section i.e., transmission zeros, of the active LC ladder filter. It is the function of the zeros or the numerator of the transfer function that determines the stopband characteristics. Balance of tank elements is critical to attain resonance. Power loss in a non–ideal inductor is usually represented by a series resistance [36] and the loss of notch depth is a result of energy leaking from the tank to the output and the reduction of signal attenuation.

A final response anomaly is reflected by the rise in gain at the magnitude passband edge. This error is also clearly reflected in the peaking of the group delay response. This characteristic response is governed by the dominant, complex–conjugate poles of the system. Figure 31 shows a plot of the filter's poles and zeros in the *s* plane. The dominant poles of the transfer function are defined as

$$p_1,\ p_2 = -\frac{\omega_o}{2Q} \pm j\omega_o\sqrt{1-\frac{1}{4Q^2}} \quad .$$

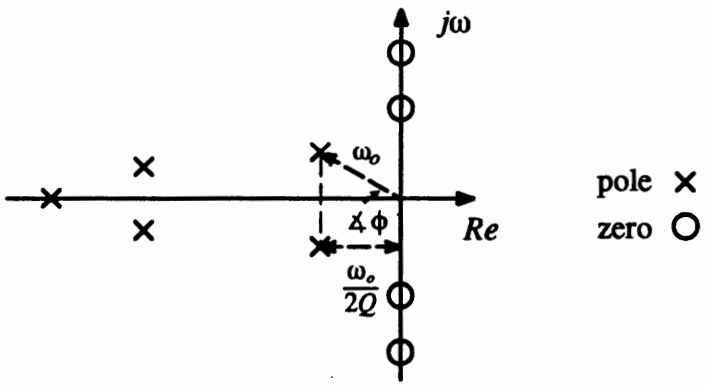


Figure 31. Fifth–order pole–zero plot

Q, the pole quality factor, determines the distance of the poles from the $j\omega$–axis and is increasing with increasing height of the 'bump' at the passband edge. Q is defined by,

$$Q = \frac{\omega_o}{2\,\mathrm{Re}[p_1]} = \frac{\sqrt{\mathrm{Re}[p_1]^2 + \mathrm{Im}[p_1]^2}}{2\,\mathrm{Re}[p_1]} = \frac{1}{2\cos\phi} \quad .$$

The magnitude and group delay peaking is caused by the excess phase shift within the circuit, and a corresponding reduction in the phase margin [33]. As the phase margin diminishes, peaking increases until the gain approaches infinity and the start of oscillation. In filters with high Q values this is a matter of great concern because the dominant pole is already close to the $j\omega$–axis and because magnitude peaking can become unacceptable. The frequency at which this peaking occurs is given by,

$$\omega_{max} \simeq \omega_o \sqrt{1 - \frac{1}{2Q^2}} \quad .$$

From TABLE I on page 17, the Q of this filter is calculated from the dominant pole to be 1.8462.

CHAPTER IV

SUMMARY AND DISCUSSION

OVERVIEW

A large quantity of data is generated in the investigative process to evaluate the device model dependence in the design of a high–frequency, analog, CMOS, transconductance–C filter. To reiterate, chapter I defined the important relationship of process parameter dependence on g_m–C filters and in a broad spectrum of related research topics. Fundamental low–pass filter particulars were reviewed to justify the response characteristics being investigated. Chapter II gave a detailed description of the methodology of investigation from the low level circuit design considerations to the high level active filter simulation techniques. Chapter III presented simulation findings in graphical and tabular formats. Observable deviant filter behavior with respect to a prototype filter response was accounted for. In this final chapter an interpretation of simulation results of the device model dependence in the design of a high–frequency, analog, CMOS, transconductance–C filter is presented. Experimental results from fabricated design are also presented. Based on these empirical findings, a discussion of the device dependence of automated analog filter design completes the chapter.

SUMMATION OF FINDINGS

Preliminary Observations of Simulation Results

Preliminary inspection of the findings in the preceding chapter reveal small variations of filter performance due to changes of process poly1/poly2 layers. Characteristic cutoff frequency varies by 1.55MHz, or 8.61%. Group delay peaking frequency variation is by the same amount. With respect to the two other simulation sets evaluated, this variation is reduced. This is because the variation of the poly1/poly2 capacitors are quite small between process runs and have a correspondingly smaller effect on overall filter performance than do MOSFET device model variations. Envelope characteristics will therefore be defined using the process *V*ariable MOSFET *M*odel with a *F*ixed value of *C*apacitance, (VMFC), and the process *V*ariable MOSFET *M*odel with a process *V*ariable *C*apacitance value, (VMVC). This decision is consistent with common computer simulation practice. Capacitance values are normally defined by a constant value, whereas active device models are often a performance dependent variable.

In a digital technology model classification system, performance is often described in terms of 'fast' or 'slow' device models [37]. It is possible to have a similar classification for MOSFETs in g_m–C filters. For analog filters, performance can be a measure of frequency response. The proposed classification system ranks a device model according to its *relative* position in the frequency performance spread. Order of the device models in the response spread are compared to high–level process dependent variables and consistent, similar series of device model ranking are chosen as a basis for a predictable,

systematic classification which can be adapted to a technology file for automated active filter synthesis.

Evaluation of Transconductance Cell Parasitic Parameters

Simulation results reveal a change of parasitic capacitance values depending upon which device model is used. A summary of the simulation derived parasitic capacitance values in TABLE IX shows input capacitance variation of 15.8% from a minimum value of 32fF to a maximum of 38fF. Output capacitance varies to a lesser extent by 9.1%, ranging from 70fF to 77fF. Standard deviation for C_i displays a 5.5% variation from the mean value, while C_o displays approximately a 3.4% variation.

TABLE IX SUMMARY OF INPUT AND OUTPUT CAPACITANCE

	Mean	MIN	MAX	% Δ	STD	% Δ_{STD}
C_i (fF)	34.6	32	38	15.8	1.9	5.5
C_o (fF)	72.8	70	77	9.1	2.5	3.4
RUN ID		N25Y	N2CQ			

Recorded values show model N2CQ has the highest values, 38fF and 77fF, for C_i and C_o, respectively, while model N25Y has the more desirable lower values of 32fF and 70fF. Filter performance shows no obvious linear relationship to these values. Both device models place in the upper half of the response envelope for both sets of simulation. The strongest correlation is between output resistance, R_o, or output conductance, g_o, ($1/R_o$) and device model response. In the same manner that C_i and C_o are calculated, so too are the input and output conductance values. TABLE X shows these calculated values with process run

identification label of spread extremes shaded. Rank of g_o in the spread is included; 1=LOW, 8=HIGH.

TABLE X ORDERED OUTPUT PARAMETERS

RUN ID	N3AB	N38L	N37C	N34O	N32A	N2CQ	N2BE	N25Y
R_o (kΩ)	455.3	280	232	387	380	240	371	315
g_o (μS)	2.20	3.57	4.31	2.58	2.63	4.17	2.70	3.17
g_o Rank	1	6	8	2	3	7	4	5

	Mean	MIN	MAX	% Δ	STD	% Δ_{STD}
R_o (kΩ)	332	232	455.3	49.0	78.8	23.7
g_o (μS)	3.17	2.20	4.31		.78	

Parameter dispersion appears to be fairly uniform. Minimum to maximum variation is approximately 50% whereas the standard deviation about the mean value is approximately 25%.

Ranking in the spread for DC gain output levels show this expected correlation to the output conductance spread. As reflected by a simple voltage divider equation, higher values of g_o in the denominator yields a higher DC attenuation level. TABLE XI shows the order of DC output level (dB), in the device model spread. Process run identification labels for extreme values are shaded; 1=LOW, 8=HIGH.

TABLE XI EMPIRICAL RANK OF MOSFET MODEL DC PERFORMANCE

RUN ID	N3AB	N38L	N37C	N34O	N32A	N2CQ	N2BE	N25Y
DC VMFC	1	6	8	2	4	7	5	3
DC VMVC	1	6	8	2	4	7	5	3

Summation of Performance Envelope Definition

Using the cutoff frequency, F_c, as a reference point, the spread order of observed points for the corresponding VMFC and the VMVC simulation sets are listed in TABLE XII; 1=LOW, 8=HIGH.

TABLE XII EMPIRICAL RANK OF MOSFET MODEL FREQUENCY PERFORMANCE

RUN ID	N3AB	N38L	N37C	N34O	N32A	N2CQ	N2BE	N25Y
F_c VMFC	1	6	8	3	4	7	2	5
F_c VMVC	1	6	8	2	4	7	3	5

The envelope of the magnitude response for the two sets of simulation being evaluated are shown in Figures 32 and 33. Mid spread order variations are not considered significant.

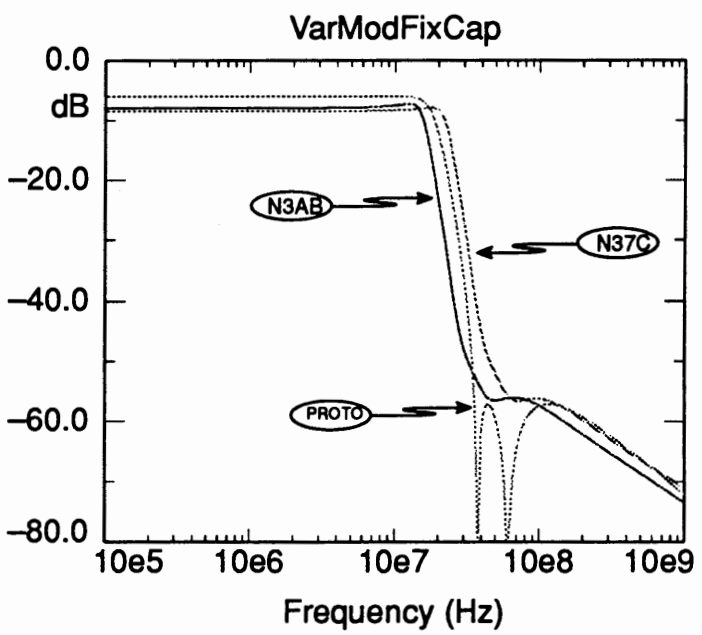


Figure 32. Envelope of magnitude response – VMFC

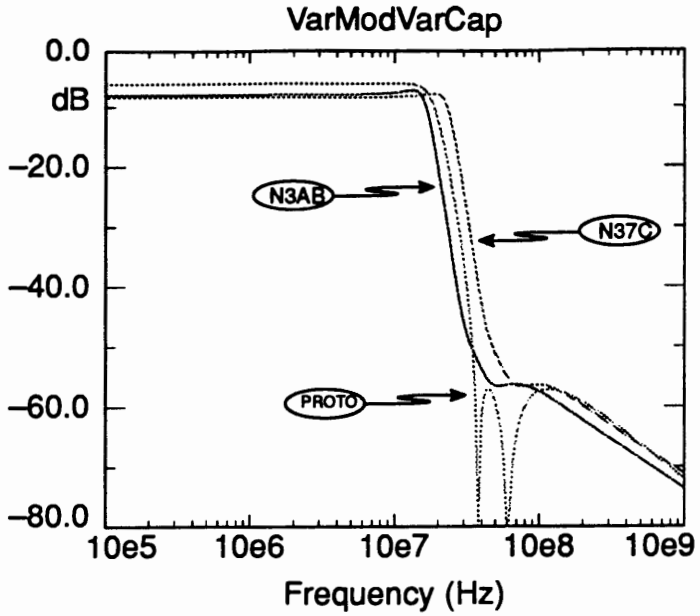


Figure 33. Envelope of magnitude response – VMVC

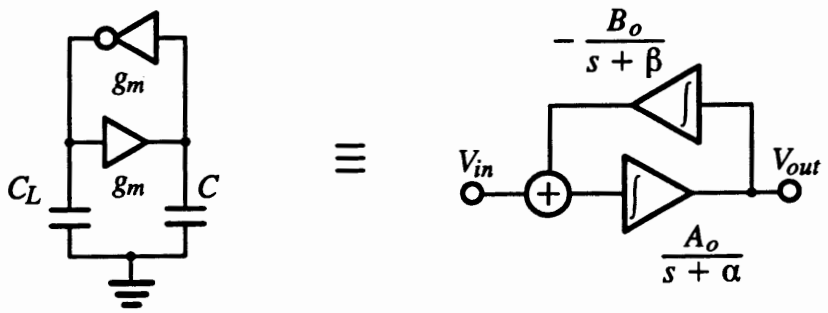
It is quite clear from the values in TABLE X and the corresponding model's ordinal placement in TABLE XII that a near direct mapping of output conductance, g_o, or output resistance, R_o, to active filter performance can be found. This result is explained quite simply by referring to the integrator characteristic equation [18] which includes parasitic components,

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m}{sC + sC_i + sC_o + g_o + g_i} \quad .$$

Consider now only a small section of the final active filter shown in Figure 13 on page 24. This section is repeated in Figure 34(a). Utilizing predistortion methods to absorb the parasitic capacitances, and neglecting g_i, the equation for a single lossy integrator reduced to,

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m}{sC + g_o} \quad .$$

By including a second inverting integrator in the feedback loop, a lossy equivalent circuit as shown in Figure 34(b) can be employed to describe the output conductance effect on filter performance;



(a) (b)

Figure 34. Two–integrator loop configuration: (a) g_m–C, (b) integrators

$$V_{out}(s) = \frac{A_o}{s+\alpha}\cdot\left(V_{in}(s) - \frac{B_o}{s+\beta}\ V_{out}(s)\right) ,$$

$$V_{out}(s)\left(1 + \frac{A_oB_o}{(s+\alpha)(s+\beta)}\right) = \frac{A_o}{s+\alpha}\cdot V_{in}(s) ,$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{A_o}{s+\alpha}}{\left(1 + \frac{A_oB_o}{(s+\alpha)(s+\beta)}\right)} ,$$

or

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{A_o(s+\beta)}{(s^2 + (\alpha+\beta)s + \alpha\beta + A_oB_o)} .$$

Making the appropriate substitutions,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_{mA}(sC + g_{oB})}{(s^2CC_L + (g_{oA}C + g_{oB}C_L)s + g_{oA}g_{oB} + g_{mA}g_{mB})} \quad .$$

From this derivation, it is clear that the cutoff frequency increases with the addition of the output conductance and that ω_o or the pole frequency moves to

$$\omega_o \simeq \sqrt{\frac{g_{mA}g_{mB} + g_{oA}g_{oB}}{CC_L}} \simeq \omega_{oideal}\sqrt{1 + \frac{g_{oA}g_{oB}}{g_{mA}g_{mB}}} \quad .$$

Pole Q is also well defined and shown to decrease,

$$Q \simeq \frac{\sqrt{g_{mA}g_{mB} + g_{oA}g_{oB}}}{g_{oA}C + g_{oB}C_L}\sqrt{CC_L} \quad .$$

The maximum Q enhancement induced bump in the magnitude, in any of the simulations, was approximately 0.5dB.

High–frequency phase response for the simulated active filter is bounded by the same device models as in the envelope of magnitude response. Both models, N3AB and N37C, show excess phase lag characteristics relative to the LC prototype response. However, in the spread of process device models, model N3AB bounds the leading phase side, whereas N37C bounds the lagging phase edge. The envelope of the phase response for the two simulations being evaluated are shown in Figures 35 and 36.

The loss of the zero effects is clearly observable as the phase plots show no distinguishable 180° phase shifts as expected or as are modeled in the prototype phase response. (The 360° shifts are due to the range of the arctan function only and should not be confused with a variation in filter phase response.)

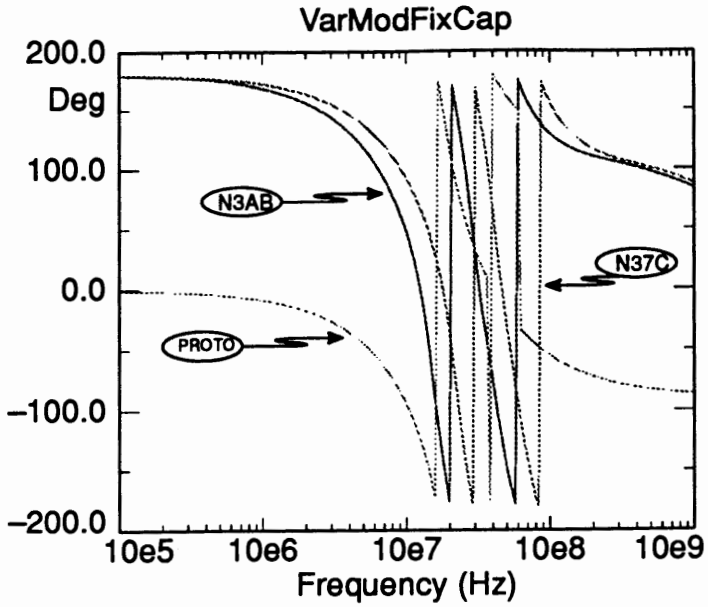


Figure 35. Envelope of phase response – VMFC

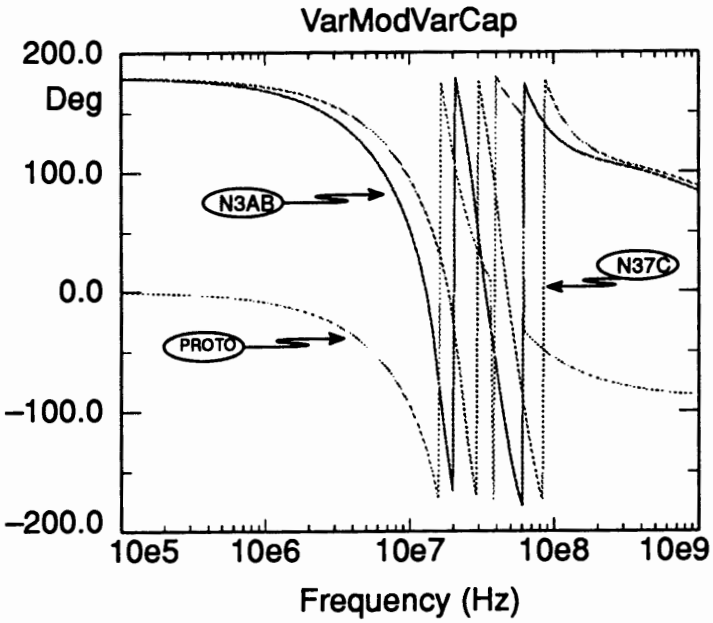


Figure 36. Envelope of phase response – VMVC

The final response characteristic investigated is the group delay response of the active filter. The envelope models are the same as in the previous two cases. This group delay response is displayed in Figures 37 and 38. Here again process run N3AB demarcates the lower extreme with a lower peaking frequency and a higher Q enhanced peaking error. Process run N37C defines the upper extreme of the linear delay frequency range and has a smaller Q enhanced peaking error. Unlike the phase response, the LC prototype response is confined to the center region. This would imply that it is more practical to compare group delays of the active filters and the LC prototype than it is to compare phase.

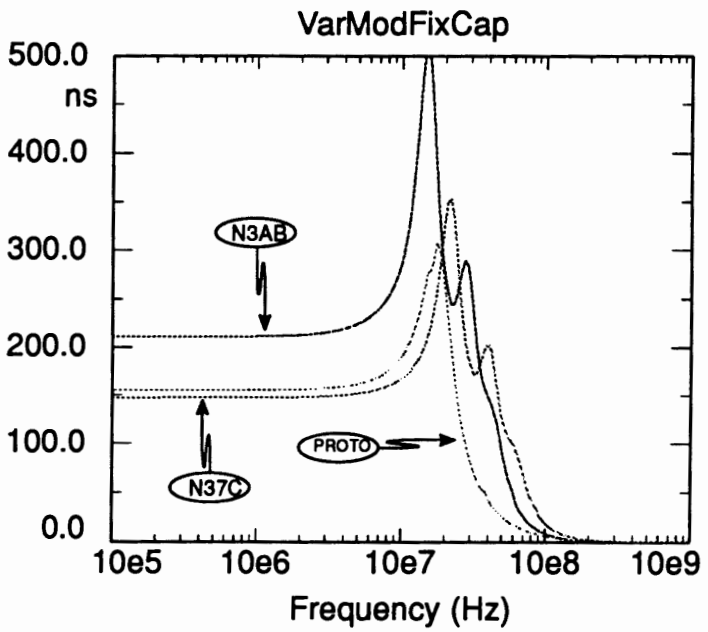


Figure 37. Envelope of group delay response – VMFC

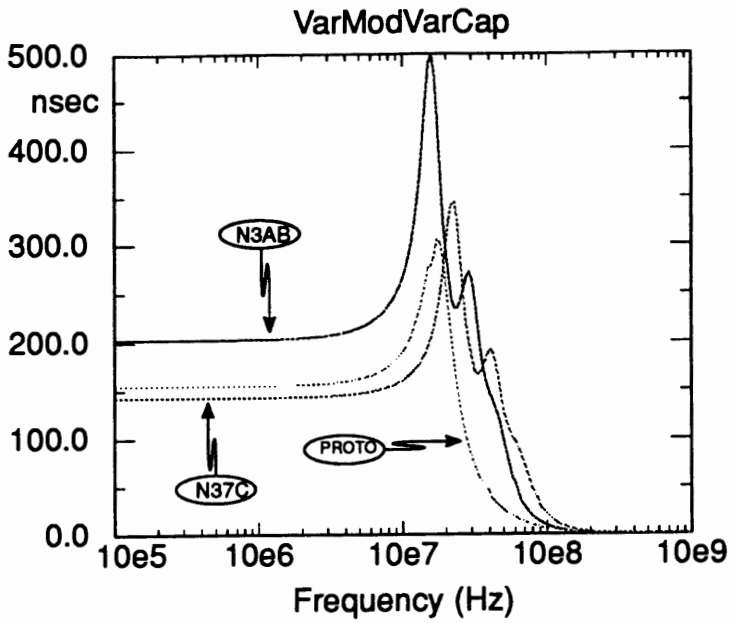


Figure 38. Envelope of group delay response – VMVC

EXPERIMENTAL RESULTS

Fabrication of the 5th–order inverse Chebyshev filter used a MOSIS SCNA, n–well, 2–poly, 2μm process. Figure 44 on page 89, shows the chip layout geometry. One single–ended filter, including DC offset nulling and output buffer circuitry, (0.650μm^2), was duplicated four times on one MOSIS TinyChip, 40 pin DIP, (4.995μm^2).

The filter performance parameters were measured with an HP 4194A Impedance/Gain–Phase Analyzer. Single–ended filter performance results are listed in TABLE XIII. Cutoff frequency of the filter as shown in Figure 39 is approximately 18 MHz. Transmission zero notches are not clearly observable. Stopband attenuation at 36MHz is measured to be –34dB. Stopband frequency at –40dB attenuation is about 41MHz. PSRR is measured to be 64dB.

TABLE XIII EXPERIMENTAL RESULTS SINGLE–ENDED FILTER

Parameter	Specification	Measured
cutoff frequency	18MHz	18MHz
passband ripple	0 dB	$\leqslant$ 1 dB
stopband frequency	36MHz	(36MHz) 41Mhz
stopband gain	$\geqslant$–40dB	(–34dB) –40dB
power supply	±5V	±2.5V→±5V
THD	<1%	not measured
SN	>40dB	>56dB
PSRR	...	64dB
power (Vdd=5V)	120mW	110mW
active filter area	...	0.438μm^2

Differential performance was easily adapted by using an unbalanced primary to balanced secondary, center–tapped transformer for the input to a pair of single–ended filters. Output was converted back to a single–ended form in

the same manner. Differential measured results are listed in TABLE XIV. Cutoff frequency of the filter as shown is Figure 40 is measured to be approximately 18MHz. Transmission zero notches are not clearly observable. Stopband attenuation at 36Mhz is measured to be about –38 dB. Stopband frequency at –40dB attenuation is approximately 39MHz. PSRR shows an expected improvement over the single–ended filter, and is measured to be 90dB.

TABLE XIV EXPERIMENTAL RESULTS DIFFERENTIAL FILTER

Parameter	Specification	Measured
cutoff frequency	18MHz	18MHz
passband ripple	0 dB	≈1dB
stopband frequency	36MHz	(36MHz) 39MHz
stopband gain	⩾–40dB	(–38dB) –41dB
power supply	±5V	±2.5V→±5V
THD	<1%	not measured
SN	>40dB	60dB
PSRR	...	90dB
power (Vdd=5V)	120mW	110mW
active filter area	...	0.948μm^2

Device model parameters for this process run N43B are listed in TABLE XVI in Appendix A. Simulation using this model results in an output conductance g_o of 2.51μS, which would predictably place it in lower end of the device model envelope.

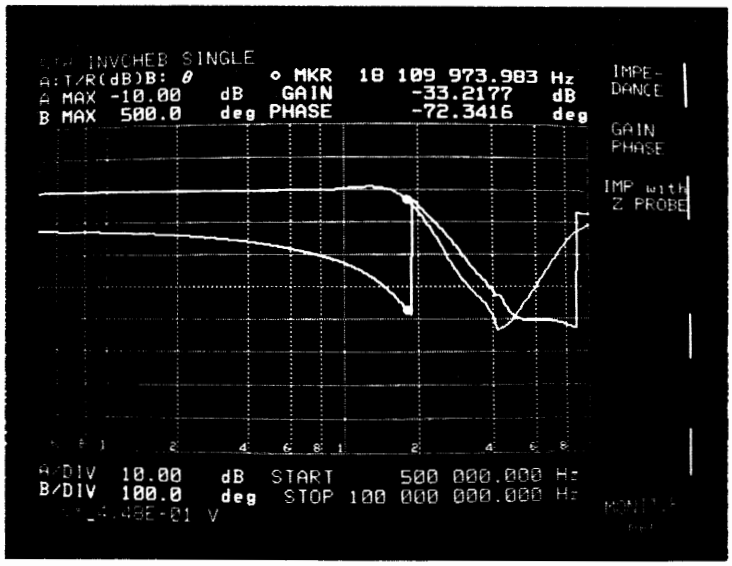


Figure 39. Experimental single–ended, active fifth–order inverse Chebyshev filter magnitude and phase response

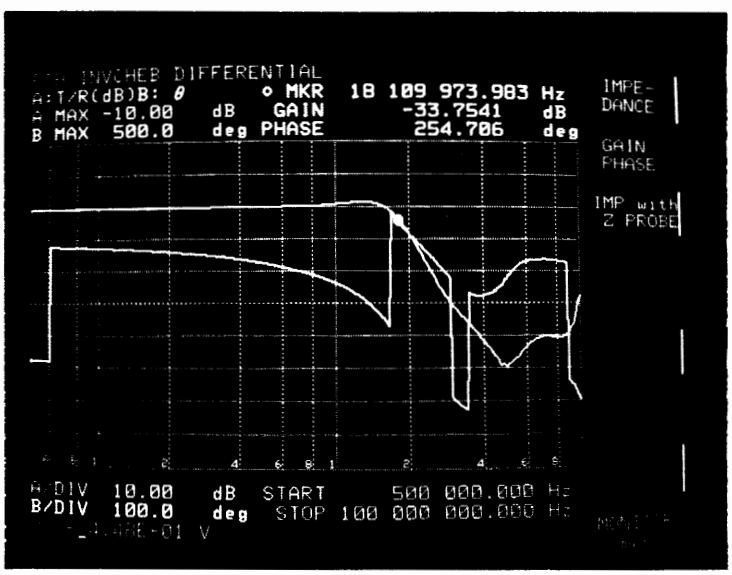


Figure 40. Experimental differential, active fifth–order inverse Chebyshev filter magnitude and phase response

DISCUSSION OF FINDINGS

The configuration of this filter using transconductance cells plays a large role in the overall filter performance. Internal to the envelope, waveform distortion is dominated by inherent disadvantages of the single–ended component structure. The remedy for this drawback is simply a matter of moving to a differential design; which is not a particularly difficult task [18] or by the techniques shown in the previous section. Elements can still be single–ended in nature, however, filter configuration is such that the additional nodes not in the LC ladder prototype can be accounted for.

Simulation phase lag characteristics are as expected due to the lossy integrators. The lack of an obvious correlation of parasitic capacitance to frequency response order in the envelope would imply that the predistortion method used in the automated filter synthesis process is quite effective for the low Q filter examined. In the discrete LC ladder structure, delay variations caused by echoes can be equalized by adding amplitude replicas of the signal derived from a tapped delay line. For active LC ladder simulation this method, though not quite as obvious, is possible to implement and further investigation of compensation methods would be worthwhile.

For the simulation set comprised of the fixed MOSFET model and variable poly1/poly2 capacitance, bounding device models were not related to extreme values of the poly1/poly2 capacitance. This would imply that the more significant contribution to filter performance is on the transconductance process dependent variables, ie MOSFETS, and not capacitance values. To minimize these less significant effects even further, the development of a technology dependent file

can incorporate such capacitor process variations and maximize accuracy by averaging process variations. Process variation trends can also be evaluated and educated "guestimates" incorporated into the process of design automation.

CONCLUSION

The purpose of this research is to evaluate device model dependence in the design of high–frequency, analog, CMOS transconductance–C filters. It is demonstrated that a high level model sort can predict the response performance of a filter with some degree of accuracy. Although individual process device parameters may always produce variable response characteristics, the worst case can be designed for to include these variations. This information may be quite useful for optimization techniques employed for increasing the yield of fabricated integrated filter designs and in design automation.

Electronic tuning is performed on the final simulated filter design to observe the magnitude of g_m tuning required to bring the response into specification. Knowing this value offers a key to the tuning problem. Although automated tuning is preferred, if a voltage can be expected for a given process variation then it can also be included in the design using standard bias generation techniques.

There is no reason to suspect that the findings of this study would not be applicable to any g_m–C filter of similar function and method of realization. Further investigation could include high Q and biquad filter designs. Benchmark tests to assist analog circuit designers with MOSFET model selection and acceptance has recently been introduced [38]. Device model dependence in the design of high–frequency, analog, bipolar and BiCMOS active filter realization could also be evaluated. The ability to predict the response spread to a predefined envelope can identify realistic tuning requirements with possible reduction in circuit complexity and size. That is, knowing the high and low limits of expected filter performance, coarse tuning strategies could be

refined. The definition of an envelope, bounded by device model extremes, can aid in the design of analog filters just as worst case design technique has benefited digital technology design.

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APPENDIX A

SPICE MODEL PARAMETERS

TABLE XV MOSIS SPICE LEVEL 2 MOSFET MODEL PARAMETERS

Part 1 of 3

PROCESS PARAMTER	RUN N3AB NMOS	RUN N3AB PMOS	RUN N38L NMOS	RUN N38L PMOS	RUN N37C NMOS	RUN N37C PMOS	RUN N34O NMOS	RUN N34O PMOS	Units
VTO V_t	0.8410	−0.9297	0.8123	−0.9901	0.8673	−0.9506	0.8466	−0.8912	V
KP $\mu_o \cdot C_{ox}$	4.6856E−05	1.6994E−05	4.6869E−05	1.6549E−05	4.6728E−05	1.6454E−05	4.7395E−05	1.6787E−05	A/V^2
GAMMA γ	0.4977	0.7262	0.4675	0.6810	0.4655	0.6561	0.4499	0.6731	$V^{.5}$
UO μ_o	569.9	206.7	568.7	200.8	569.7	200.6	554.5	196.4	$cm^2/V \cdot s$
TOX t_{ox}	4.2000E−08		4.1900E−08		4.2100E−08		4.0400E−08		m
NSUB N_A, N_D	5.0450E+15	1.0740E+16	4.4720E+15	9.4900E+15	4.3910E+15	8.7250E+15	4.4540E+15	9.9710E+15	$1/cm^3$
LAMBDA λ	3.1750E−02	4.4380E−02	3.3370E−02	4.5130E−02	3.9720E−02	4.5950E−02	3.0810E−02	4.0620E−02	1/V
XJ X_j	0.2000U		0.2000U		0.2000U		0.2000U		m
DELTA Δ	6.0220	3.8240	5.5710	5.2390	4.9450	4.5950	5.9610	5.2050	–
LD L_d	7.3030E−08	3.3390E−07	3.0410E−07	3.8900E−07	3.5223E−07	3.7200E−07	2.0100E−07	2.5600E−07	m
UEXP U	2.2470E−01	2.6190E−01	1.4610E−01	2.9100E−01	1.7090E−01	2.6690E−01	1.3210E−01	3.2050E−01	–
UCRIT $\mathcal{E}_c$	8.3850E+04	8.6610E+04	8.6360E+04	8.4920E+04	5.9350E+04	7.9260E+04	8.2580E+04	1.0330E+05	V/cm
RSH	2.0000E+01	5.7120E+01	2.1170E+01	4.8190E+01	1.9090E+01	4.9920E+01	2.2460E+01	5.2420E+01	ohm/Sq
NFS	1.980E+11	3.270E+11	1.9800E+11	3.270E+11	1.9800E+11	3.270E+11	1.98E+11	3.27E+11	$1/cm^2$
VMAX v_{max}	6.6330E+04	9.9990E+05	5.9890E+04	9.9990E+05	5.7510E+04	9.9990E+05	5.7310E+04	9.9990E+05	m/s
CGDO/GSO	9.0065E−11	4.1179E−10	3.7593E−10	4.8089E−10	4.3332E−10	4.5769E−10	2.5770E−10	3.2822E−10	F/m
CGBO	4.8051E−10	3.6700E−10	3.9487E−10	3.7299E−10	3.5977E−10	3.8123E−10	3.9810E−10	4.0267E−10	F/m
CJ C_{j0}	9.1203E−05	3.1278E−04	9.2516E−05	3.2306E−04	1.0096E−04	3.1469E−04	9.3197E−05	3.1819E−04	F/m^2
MJ n	0.7451	0.5709	0.7551	0.5717	0.8119	0.5687	0.8129	0.5596	–
CJSW C_{jsw0}	2.4684E−10	3.4621E−10	4.8928E−10	3.0368E−10	4.6983E−10	3.1456E−10	4.6232E−10	3.0374E−10	F/m
MJSW n	0.068631	0.294506	0.336658	0.259043	0.323107	0.275802	0.317442	0.261342	–

TABLE XV MOSIS SPICE LEVEL 2 MOSFET MODEL PARAMETERS

Part 2 of 3

PROCESS PARAMTER	RUN N32A NMOS	PMOS	RUN N2CQ NMOS	PMOS	RUN N2BE NMOS	PMOS	RUN N25Y NMOS	PMOS	Units
VTO V_t	0.8630	−0.9629	0.8785	−0.9328	0.8236	−0.9584	0.825008	−0.937048	V
KP $\mu_o \cdot C_{ox}$	4.7401E−05	1.7106E−05	4.5097E−05	1.6211E−05	4.5744E−05	1.5386E−05	4.9190E−05	1.7310E−05	A/V^2
GAMMA γ	0.4374	0.6180	0.3855	0.7040	0.5049	0.7510	0.172	0.715	$V^{.5}$
UO μ_o	562.8	203.1	547.2	196.7	552.4	185.8	594	209	$cm^2/V{\cdot}s$
TOX t_{ox}	4.1000E−08		4.1900E−08		4.1700E−08		417.00E−10		m
NSUB N_A, N_D	4.0880E+15	8.1610E+15	3.0400E+15	1.0140E+16	5.2670E+15	1.1650E+16	6.1086E+14	1.0561E+16	$1/cm^3$
LAMBDA λ	3.1840E−02	4.5120E−02	3.6530E−02	4.5280E−02	2.9840E−02	4.2020E−02	6.6362E−03	4.3914E−02	1/V
XJ X_j	0.200000U		0.250000U		0.250000U		0.250000U		m
DELTA Δ	6.6420	5.7540	8.1630	5.1380	5.1270	3.6660	5.0831	1.0718	–
LD L_d	2.4780E−07	3.0910E−07	3.6430E−07	4.3980E−07	1.8070E−07	3.1970E−07	2.5000E−07	2.2724E−07	m
UEXP U	1.5270E−01	2.1320E−01	1.5620E−01	2.9080E−01	1.5150E−01	3.0820E−01	6.6823E−02	0.233831	–
UCRIT $\mathcal{E}_c$	7.7040E+04	8.0280E+04	7.4490E+04	8.6500E+04	9.2630E+04	1.0260E+05	0.5000E+04	4.7510E+04	V/cm
RSH	2.4000E+01	5.6770E+01	2.3660E+01	5.4470E+01	2.6550E+01	5.1080E+01	3.2740E+01	7.2960E+01	ohm/Sq
NFS	1.980E+11	3.270E+11	1.98E+11	3.27E+11	1.9800E+11	3.270E+11	1.98E+11	3.27E+11	$1/cm^2$
VMAX $\mathcal{V}_{max}$	5.8030E+04	9.9990E+05	5.8270E+04	2.4900E+05	5.8570E+04	9.9990E+05	6.5547E+04	1.000E+05	m/s
CGDO/GSO	3.1306E−10	3.9050E−10	4.5035E−10	5.4368E−10	2.2445E−10	3.9711E−10	3.1053E−10	2.8226E−10	F/m
CGBO	4.3449E−10	4.1280E−10	3.9262E−10	3.8703E−10	3.9785E−10	3.9682E−10	3.8485E−10	5.2924E−10	F/m
CJ	9.5711E−05	3.2437E−04	7.0260E−05	3.2050E−04	9.1699E−05	3.2659E−04	9.4949E−05	3.2242E−04	F/m^2
MJ	0.7817	0.5637	0.6906	0.5683	0.8283	0.5680	0.847099	0.584956	–
CJSW	5.0429E−10	3.3912E−10	4.7672E−10	3.1339E−10	4.1092E−10	3.1624E−10	4.4101E−10	2.9791E−10	F/m
MJSW	0.346510	0.275876	0.332090	0.272128	0.297720	0.260598	0.334060	0.310807	–

TABLE XV MOSIS SPICE LEVEL 2 MOSFET MODEL PARAMETERS

Part 3 of 3

PROCESS PARAMTER	ALL RUNS NMOS	PMOS				Units
PHI $2\phi_f$	0.6000					V
PB ψ_0	0.8000					V
TPG	1	−1				–

TABLE XVI MOSIS SPICE LEVEL 2 PARAMETERS: EXPERIMENTAL MODEL

Part 1 of 2

PROCESS PARAMTER	RUN N43B NMOS	PMOS				Units
VTO V_t	0.8109	−1.0600				V
KP $\mu_o \cdot C_{ox}$	4.8109E−05	2.2267E−05				A/V^2
GAMMA γ	0.4512	0.3746				$V^{.5}$
UO μ_o	593.5	274.7				$cm^2/V \cdot s$
TOX t_{ox}	4.260E−08					m
NSUB N_A, N_D	4.0300E+15	2.7770E+15				$1/cm^3$
LAMBDA λ	2.62100E−02	5.3990E−02				1/V
XJ X_j	0.200000U					m
DELTA Δ	6.7500	9.0900				–
LD L_d	9.2070E−08	1.7890E−07				m
UEXP U	1.4990E−01	3.4430E−01				–
UCRIT $\mathcal{E}_c$	8.1140E+04	6.9200E+04				V/cm
RSH	2.4540E+01	5.9420E+01				ohm/Sq
NFS	1.98E+11	3.23E+11				$1/cm^2$
VMAX V_{max}	6.2580E+04	9.9990E+05				m/s
CGDO/GSO	1.1195E−10	2.1752E−10				F/m
CGBO	4.7024E−10	3.9953E−10				F/m
CJ C_{j0}	1.0922E−04	3.1585E−04				F/m^2
MJ n	0.8608	0.5914				–
CJSW C_{jsw0}	2.4755E−10	3.2974E−10				F/m
MJSW n	0.035834	0.315516				–

TABLE XVI MOSIS SPICE LEVEL 2 PARAMETERS: EXPERIMENTAL MODEL

PROCESS PARAMTER	RUN N43B NMOS	PMOS				Units
PHI $2\phi_f$	0.6000					V
PB ψ_0	0.8000	0.7000				V
TPG	1	−1				–

Notes:

POLY1/POLY2 Capacitance: fF/μm^2=0.457, fF/Tile=49.360

APPENDIX B

SPICE SIMULATION TEST CODE

Spice Simulation Test Code

```
* file: spsh
* ALTERATIONS TO DECK
* IOUT1  +(vt)– IOUT  dummy voltage source, (ammeter)
* model selection, global substitutions in deck file
*    %s/nfetLL/nfetLL/g
*    %s/pfetLL/pfetLL/g
.include model.file
.include 20x8invgm.spice
*  OR
*.include 20x8if.spice
.include dcoff20x8.spice
***Power supplies
Vvdd Vdd 0  5v
Vvss  Vss 0 –5v
Vgnd GND 0 0v
VVGPOS VGPOS 0  dc=3.75
VVGNEG VGNEG 0  dc=–3.75
Vvc VC 0 dc=0
** For GmCell Measurements
** INPUT
vvin VIN 0 ac .5 sin(0 .5 1e9 0 0) dc=0
*** LOADED ****
* AMMETER ON THE OUTPUT
vt IOUT1 IOUT dc=0
** For Ci & Co measurements  Do LOW & HIGH Frequency
**** Ci, Ri,  plot imag(i(vvin)/(frequency*2*pi*vin))  vin/(re(i(vvin)))
* vvin VIN 0 ac .5 sin(0 .5 1e9 0 0) dc=0
* vt IOUT 0 dc=0
**** Co, Ro plot imag(i(vt)/(frequency*2*pi*IOUT))  IOUT/(re(i(vt)))
* vvin VIN 0 dc=0
* vt IOUT 0 ac .5 sin(0 .5 1e9 0 0) dc=0
** INTERACTIVE COMMANDS
```

```
.dc vvin –2 2 .01
* plot i(vt), plot iout, plot  –deriv(i(vt))
*.ac dec 50 100k 100gig
*.ac dec 50 .1 100
* plot –db(i(vt)/vin) * plot iout/i(vt) output resistance
* show * op > gm.results * tf i(vt) vvin
.end


** SPICE file created for circuit 20x8invgm Grounded Resistor Configuration **
** Technology: scmos
*
M0 Vdd VGPOS 6_284_226 Vss              nfetLL L=2.0U W=8.0U
M1 IOUT IOUT 6_308_226 Vss              nfetLL L=2.0U W=8.0U
M2 IOUT IOUT 6_284_226 6_284_226        pfetLL L=2.0U W=20.0U
M3 Vss VGNEG 6_308_226 VBOFF            pfetLL L=2.0U W=20.0U
*
M4 Vdd VGPOS 6_284_124 Vss              nfetLL L=2.0U W=8.0U
M5 IOUT1 Vin 6_308_124 Vss              nfetLL L=2.0U W=8.0U
M6 IOUT1 Vin 6_284_124 6_284_124        pfetLL L=2.0U W=20.0U
M7 Vss VGNEG 6_308_124 VBOFF            pfetLL L=2.0U W=20.0U
*
C0 VBOFF Vss 5F
C1 6_284_124 6_308_124 4F
C2 6_284_226 6_308_226 4F
C3 6_308_124 0 63F
C4 Vin 0 5F
C5 6_284_124 0 74F
C6 Vss 0 104F
C7 VGNEG 0 4F
C8 VBOFF 0 16F
C9 6_308_226 0 63F
C10 Vdd 0 62F
C11 IOUT 0 128F
```

```
C12 VGPOS 0 14F
C13 6_284_226 0 74F

** SPICE file created for circuit 20x8if  Inverting Gm Cell **
M0 Vdd VGPOS 6_21_268 Vss                    nfetLL L=2.0U W=8.0U
M2 IOUT Vin 6_21_268 6_21_268                pfetLL L=2.0U W=20.0U
M1 IOUT Vin 6_4_268 Vss                      nfetLL L=2.0U W=8.0U
M3 Vss VGNEG 6_4_268 VBOFF                   pfetLL L=2.0U W=20.0U
C0 6_21_268 6_4_268 4F
C1 Vss 0 53F
C2 VBOFF 0 7F
C3 IOUT 0 61F
C4 6_4_268 0 63F
C5 Vdd 0 32F
C6 Vin 0 5F
C7 VGPOS 0 14F
C8 6_21_268 0 74F


** SPICE file created for circuit dcoff20x8  Bulk Bias Generator **
** Technology: scmos
M90 Vdd VGPOS 6_332_394 Vss                  nfetLL L=2.0U W=8.0U
M91 VBOFF vodc 6_356_394 Vss                 nfetLL L=2.0U W=8.0U
M92 VBOFF vodc 6_332_394 6_332_394           pfetLL L=2.0U W=20.0U
M93 Vss VGNEG 6_356_394 VC                   pfetLL L=2.0U W=20.0U
*
M94 Vdd VGPOS 6_332_292 Vss                  nfetLL L=2.0U W=8.0U
M95 vodc GND 6_356_292 Vss                   nfetLL L=2.0U W=8.0U
M96 vodc GND 6_332_292 6_332_292             pfetLL L=2.0U W=20.0U
M97 Vss VGNEG 6_356_292 VBOFF                pfetLL L=2.0U W=20.0U
*
C90 6_332_292 6_356_292 4F
C91 6_332_394 6_356_394 4F
C92 6_356_292 0 63F
C93 6_332_292 0 76F
```

C94 Vss 0 105F
C95 VGNEG 0 4F
C96 VC 0 7F
C97 VBOFF 0 72F
C98 6_356_394 0 63F
C99 Vdd 0 63F
C910 vodc 0 66F
C911 VGPOS 0 17F
C912 6_332_394 0 74F

APPENDIX C

MAGIC CELL LAYOUT

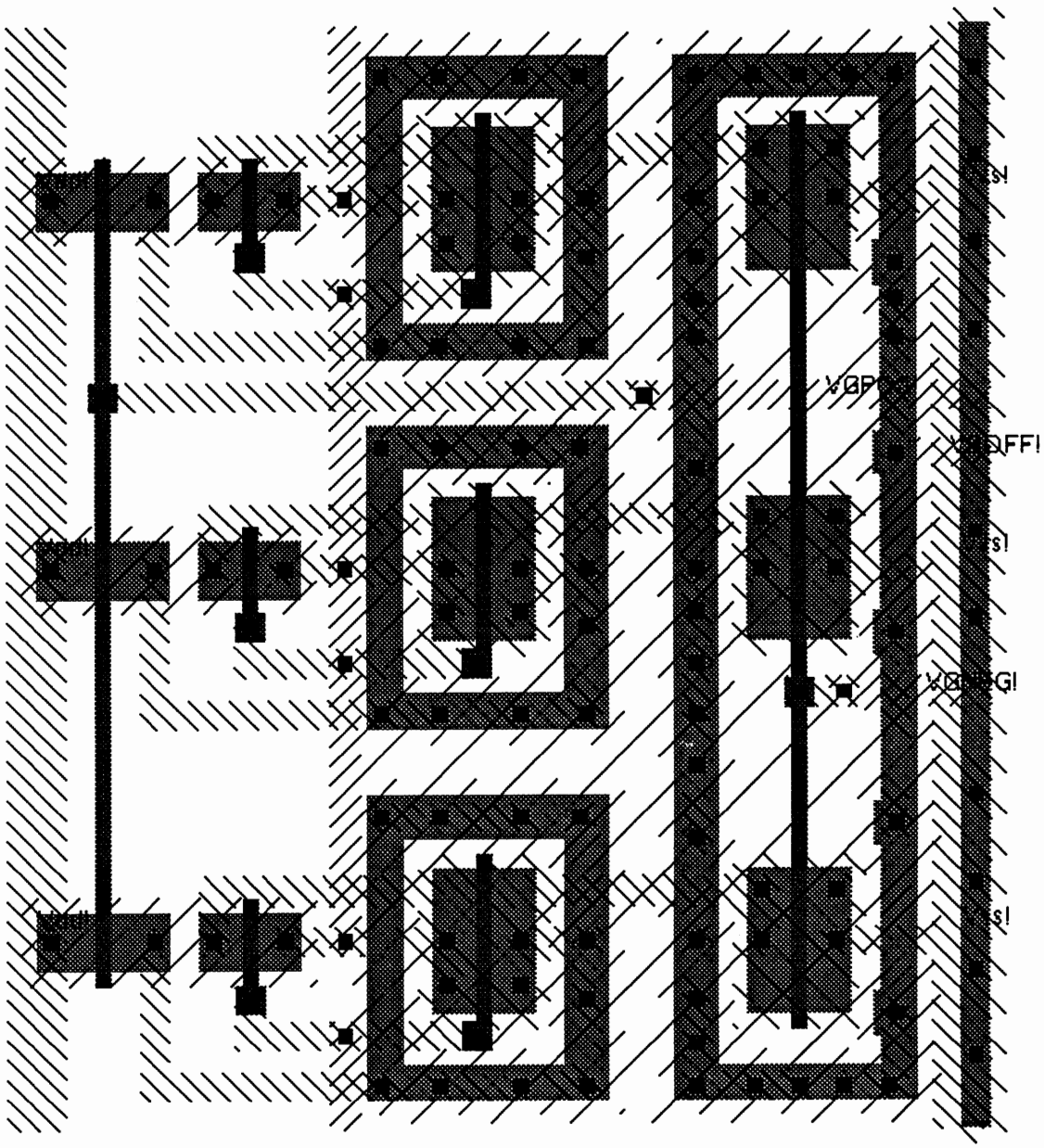

Figure 41. Non–inverting transconductance cell Magic layout

Note: All Magic layout pictures use standard black and white stipple patterns.

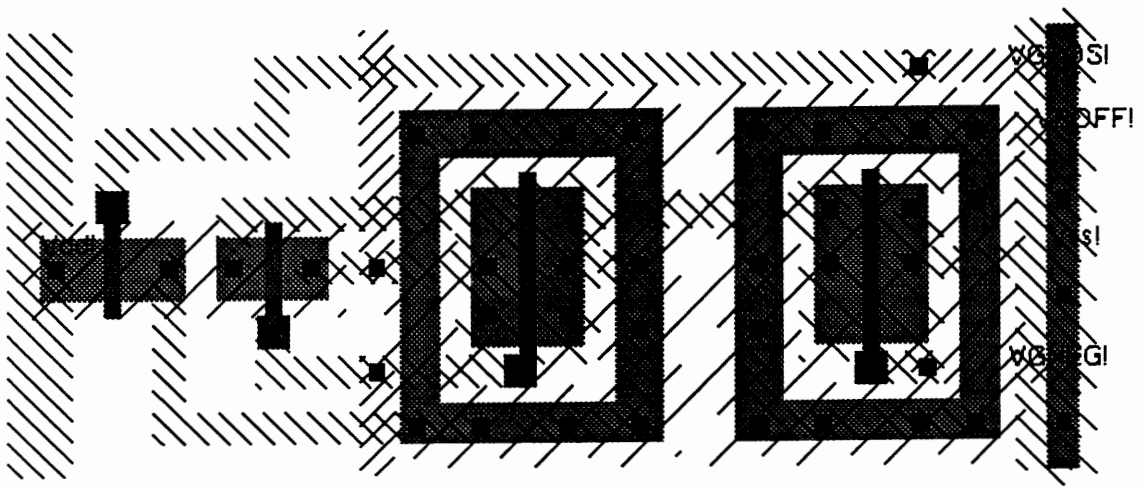

Figure 42. Inverting transconductance cell Magic layout

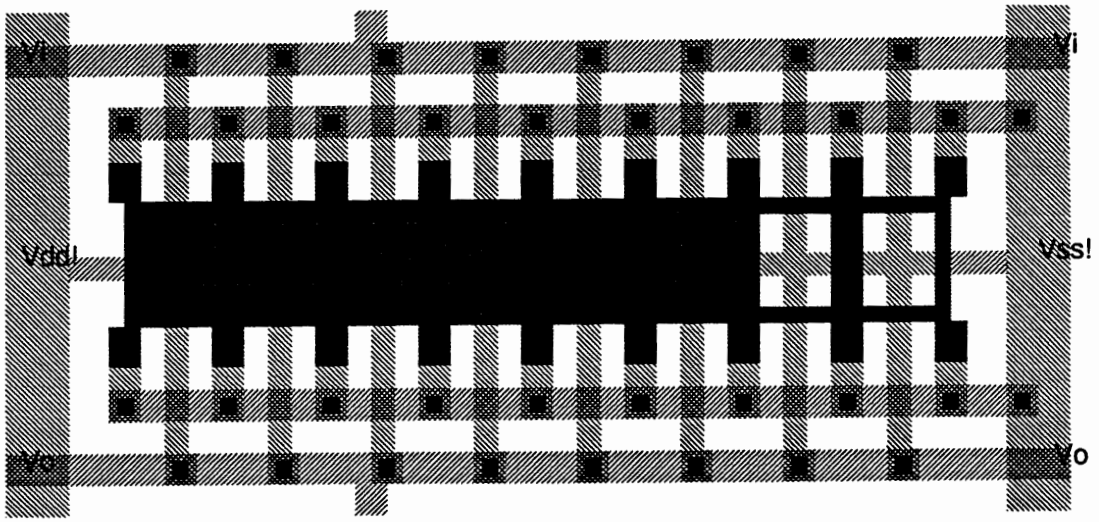

Figure 43. Grid capacitor

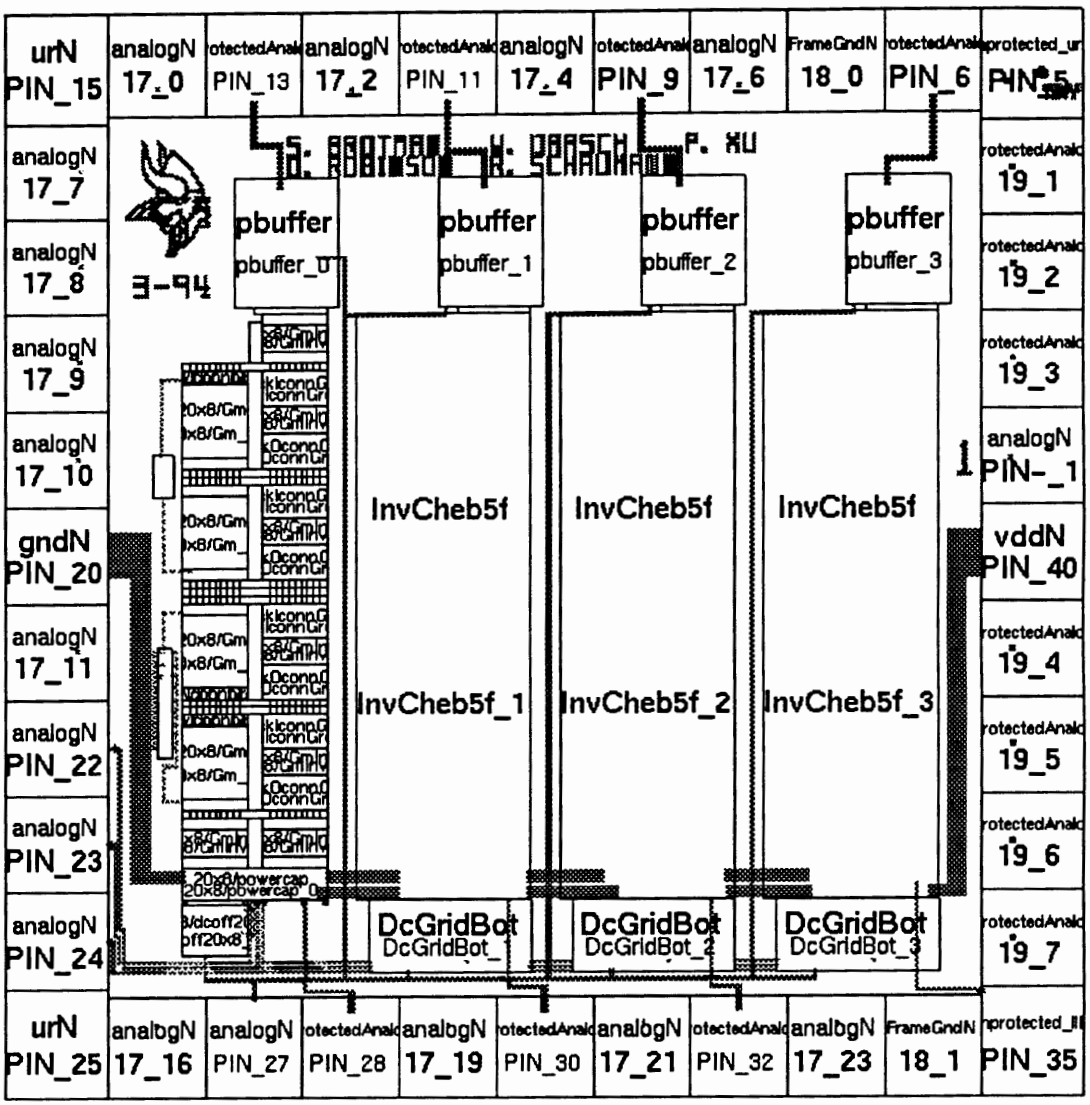

Figure 44. Final integrated circuit geometry layout

APPENDIX D

SCHEMATIC DIAGRAM

Schematic Diagram DC Bias Generator

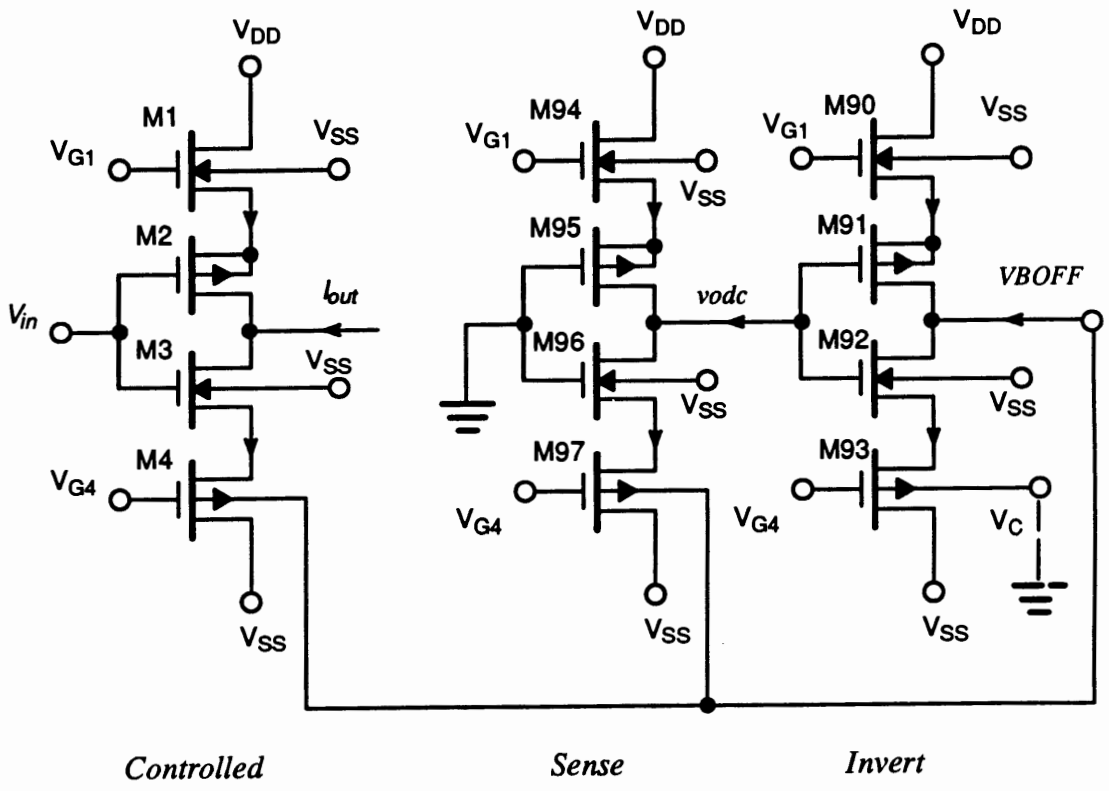

Figure 45. DC offset bias circuit

Notes:

1. The inclusion of V_c on the bulk of M93 is as an additional tuning parameter. Preliminary simulations show that this well may be left floating with no obvious effects.
2. All gate bias voltages are global to all four filters.
3. Each filter has its own DC bias generator.